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Preface

This book explores integrated gate drivers with emphasis on new GaN power transistors, which offer fast switching along with minimum switching losses. In this environment, the gate driver is a key component that enables advanced, energy-efficient, robust, and compact power electronics. As GaN transistors are relatively new, there is still a large innovation potential for suitable integrated gate drivers. IC technology enables miniaturization by scaling down length of interconnections at the power stage. As a main advantage, this reduces parasitic inductances, which allow for even faster switching such that the potential of GaN as well as of conventional Si-based switches can be utilized. Nevertheless, there are still a large number of challenges in the area of gate drivers.

The book investigates solutions on system and circuit level for highly integrated gate drivers. It includes (1) miniaturization by higher integration of subfunctions onto the IC (buffer capacitors) and (2) more efficient switching by a multilevel approach, which also improves robustness in case of extremely fast switching transitions. It presents (3) a concept for robust operation in the highly relevant case that the gate driver is placed in distance to the power transistor. All results are widely applicable.

Fast switching gate drivers require that the driver is capable of high output currents. Depending on the semiconductor technology, conventional gate drivers suffer from large die area occupied by the gate driver output stage resulting in high costs. This book introduces two concepts with various benefits such as area savings and increased driving speed: high-voltage charge storing (HVCS) and high-voltage energy storing (HVES). As a key idea of HVCS, the main bootstrap capacitor is supported by a second bootstrap capacitor that is charged to a higher voltage and ensures high charge allocation when the driver turns on. HVCS achieves ∼70 % area reduction of the bootstrap capacitor that is required to provide the charge for the pre-driver pull-up NMOS transistor of the driver output stage. Besides drivers, the proposed bootstrap circuit can also be directly applied to power stages to achieve fully integrated switched mode power supplies or class D output stages. With the current trend towards monolithic integration of gate drivers on the same die as

the GaN transistor, HVCS is very attractive to reach the integration of the buffer capacitor, achieving higher reliability, easier usage, and faster switching.

In addition to HVCS, HVES is based on a resonant behavior, basically due to an integrated inductor in the gate charge path. This enables to deliver high-current pulses based on a resonant discharging of a high-voltage buffer capacitor over this inductor to the gate. The key idea is to transfer the energy stored in the buffer capacitor to the gate, charging it, e.g., to 5 V. Since the energy in the capacitor is proportional to the square of its initial voltage (e.g., 15 V), the circuit can provide a large amount of charge on a small die area. Moreover, HVES shows a ∼25 % higher gate drive speed compared to a conventional gate driver, even at a three times larger gate loop inductance. Hence, HVES is in particular suitable for two scenarios: (1) if the inductance of the gate loop is a limiting factor for higher gate driver speed, and (2) it enables the integration of buffer capacitors capable of driving even large types of GaN transistors at an appropriate gate driver efficiency. An experimental implementation delivers up to 11 nC gate charge from a fully integrated buffer capacitor (no external components) along with a robust bipolar and three-level gate drive scheme.

Based on high-voltage energy storing, a gate driver concept and various implementation options are proposed that allow for placing the gate driver in large distance from the power transistor without sacrificing the switching performance. Experimental results show an increase in the gate drive speed of up to ∼40 %. Transient measurements show 60 V ns^{-1} steep voltage transitions at a GaN transistor, with a distance of the gate driver to the power transistor of ∼25 cm. This concept allows for different temperatures and different substrates for the gate driver and transistor, resulting in better component placement depending on application constraints.

The objective of this book is to provide a systematic and comprehensive insight into gate drive techniques for fast switching power stages. Both theoretical and practical aspects are covered. Design guidelines are derived for various gate drivers, level shifters, and supporting circuits as well as for the on-chip buffer capacitors in case of HVCS and HVES. The material will be interesting for design engineers in industry as well as researchers who want to learn about and implement gate drivers.

This book is based on our research at Reutlingen University, Reutlingen, Germany, and at the Institute for Microelectronic Systems at Leibniz University Hannover, Hannover, Germany. The work was partially sponsored by the State of Baden-Württemberg and by the Federal Ministry of Education and Research Germany (Grand No. 16ES0080). We are grateful to all team members for the invaluable support as well as the enjoyable collaboration. A special thanks goes to our families, without their love and support this book would not have been possible.

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Contents

Acronyms

List of Abbreviations

2DEG	Two-dimensional electron gas
Al	Aluminum
BCD	Bipolar complementary metal oxide semiconductor (CMOS) double-diffused metal oxide semiconductor (DMOS)
BJT	Bipolar junction transistor
CMOS	Complementary metal oxide semiconductor
CMTI	Common-mode transient immunity
DMOS	Double-diffused metal oxide semiconductor
EMC	Electromagnetic compatibility
EMI	Electromagnetic interference
FOM	Figure of merit
GaN	Gallium nitride
GIT	Gate injection transistor
HVCS	High-voltage charge storing
HVES	High-voltage energy storing
IC	Integrated circuit
IGBT	Insulated gate bipolar transistor
LDO	Linear regulator
LiDAR	Light detection and ranging
MOS	Metal oxide semiconductor
MOSFET	Metal oxide semiconductor field effect transistor
NMOS	N-channel metal oxide semiconductor
PCB	Printed circuit board
PFC	Power-factor correction
PMOS	P-channel metal oxide semiconductor
PWM	Pulse-width modulation
QFN	Quad-flat no-lead package
Si	Silicon

SiC	Silicon carbide
SJMOSFET	Superjunction MOSFET
SMD	Surface-mounted device
SOA	Safe-operating area
SOIC	Small-outline integrated circuit

List of Symbols

A	m^2	Area of the electrodes of a plate capacitor
B_p		Buffer in gate driver circuit for driving large gate loops
C_{B1}	F	Low-voltage bootstrap capacitor of the HVCS circuit
C_{B2}	F	High-voltage bootstrap capacitor of the HVCS circuit
C_{BST}	F	Bootstrap capacitor
C_{Buf}	F	Buffer capacitor (called C_{HVp} / C_{HVn} in the implemented gate driver circuits)
C_{cpl}	F	Coupling capacitance between the gate driver low-side and high-side
C_{CP}	F	Capacitor of the "V_{DRV} C_P" circuit
C_{DS}	F	Drain-source capacitance
C_{DRV}	F	Gate driver buffer capacitor
C_G	F	Total gate capacitance of the power transistor
$C_{G,eq}$	F	Equivalent linear gate capacitance
C_{GD}	F	Gate-drain capacitance
C_{GS}	F	Gate-source capacitance
$C_{GS,add}$	F	Capacitor connected in parallel to the gate-source terminals of the power transistor
C_{HVn}	F	High-voltage capacitor of the HVES circuit (transistor's source side)
C_{HVp}	F	High-voltage capacitor of the HVES circuit (transistor's gate side)
C_{HVx}	F	High-voltage capacitors of the HVES circuit (transistor's gate/source side)
CLK_{CP}	F	Clock signal of the "V_{DRV} C_P"
C_{loop}	F	Equivalent gate loop capacitance
C_{oss}	F	Output capacitance of the power transistor ($C_{GD} + C_{DS}$)
$C_{o(ER)}$	F	Effective output capacitance of the power transistor—energy related
$C_{o(TR)}$	F	Effective output capacitance of the power transistor—time related

C_P	F	Charge pump pumping capacitor
C_{plate}	F	Capacitance of a plate capacitor
d	m	Distance between the electrodes of a plate capacitor
D		Damping factor of the gate loop
D_B		Bootstrap diode of high-side gate driver supply
D_{B1}		Bootstrap diode for low-voltage supply rail of the HVCS circuit
D_{B2}		Bootstrap diode for high-voltage supply rail of the HVCS circuit
D_{C1}		Diode of the charge pump circuit
D_{C2}		Diode of the charge pump circuit
D_{clpn}		Clamping diode of the gate driver for large gate loops (transistor's source side)
D_{clpp}		Clamping diode of the gate driver for large gate loops (transistor's gate side)
D_{CP}		Diode of the charge pump circuit
D_{clp}		Clamping diode, protecting the supply-voltage input of a high-side gate driver
D_{FW}		Free-wheeling diode
D_{FWn}		Free-wheeling diode of the gate driver for large gate loops (transistor's source side)
D_{FWp}		Free-wheeling diode of the gate driver for large gate loops (transistor's gate side)
D_R		Rectifier diode of HVES circuit
D_{Rn}		Rectifier diode of HVES circuit (transistor's source side)
D_{Rp}		Rectifier diode of HVES circuit (transistor's gate side)
DRV_{IN}	V	Gate driver control signal
DRV_{INn}	V	Gate driver control signal (transistor's source side)
DRV_{INp}	V	Gate driver control signal (transistor's gate side)
ΔV_{GS}	V	Amplitude of the voltage dip of V_{GS}, caused by the Miller coupling
ϵ_r	$F\,m^{-1}$	Relative permittivity of a dielectric medium
ϵ_o		Electric constant
η		Efficiency of a turn-on event of the HVES / HVCS circuit
η_{HVES}		Efficiency of a turn-on event of the HVES circuit
E_{CBuf}	J	Energy in C_{Buf}
E_{CG}	J	Energy in C_G
E_{in}	J	Energy from C_{Buf} at driver turn-on
$E_{chargingLossCoss}$	J	Dissipated energy when charging C_{oss} from 0 V to the stated V_{DS} via an energy-dissipating element

E_{oss}	J	Energy stored in the fully charged C_{oss}
E_{loss}	J	Energy dissipated during a driver turn-on event
$E_{loss,HVES}$	J	Energy dissipated during a driver turn-on event in the HVES circuit
E_{out}	J	Energy stored in C_G after driver turn-on
E_n	J	Energy from HVES circuit at driver turn-off
E_p	J	Energy from HVES circuit at driver turn-on
f_{CP}	Hz	Clock frequency of the "V_{DRV} C_P"
I_{CP}	A	Load current of the "V_{DRV} C_P" circuit
I_D	A	Drain current of the power transistor
I_L	A	Load current
I_n		Inverter in the gate driver circuits for driving large gate loops
I_{peak}	A	Peak driver output current
I_G	A	Gate drive current
$I_{G,sink}$	A	Sink gate drive current
$I_{G,sink,max}$	A	Maximum sink gate drive current
$I_{G,source}$	A	Source gate drive current
$I_{G,source,max}$	A	Maximum source gate drive current
k_1		Scaling factor of C_{B1} accounting for process tolerances
k_2		Scaling factor of C_{B2} accounting for process tolerances
$k_{1,max}$		Maximum specified scaling factor of C_{B1} accounting for process tolerances
$k_{2,max}$		Maximum specified scaling factor of C_{B2} accounting for process tolerances
$k_{1,min}$		Minimum specified scaling factor of C_{B1} accounting for process tolerances
$k_{2,min}$		Minimum specified scaling factor of C_{B2} accounting for process tolerances
L	H	Inductor as part of the equivalent HVES circuit (called L_{HVp} / L_{HVn} in the implemented gate driver circuits)
L_{HV}	H	Inductor as part of the HVES circuit
L_{HVn}	H	Inductor of the HVES circuit (transistor's source side)
L_{HVp}	H	Inductor of the HVES circuit (transistor's gate side)
L_{HVx}	H	Inductor of the HVES circuit (transistor's gate/source side)
L_{loop}	H	Gate loop inductance
L_{par}	H	Parasitic inductance
$LSin$	V	Level-shifter input signal
$LSout$	V	Level-shifter output signal

M_{CP}		Low-voltage transistor of the "CHV C_P" circuit
M_{CP2}		High-voltage transistor of the "V_{DRV} C_P" circuit
M_{Hn}		High-voltage transistor of the gate driver for large gate loops (transistor's source side)
M_{HVn}		High-voltage transistor of the gate driver based on HVES (transistor's source side)
M_{Hp}		High-voltage transistor of the gate driver for large gate loops (transistor's gate side)
M_{HVp}		High-voltage transistor of the gate driver based on HVES (transistor's gate side)
M_{HVx}		High-voltage transistor M_{HVp} or M_{HVn}
M_{Lp}		High-voltage transistor of the gate driver for large gate loops (transistor's gate side)
M_{Ln}		High-voltage transistor of the gate driver for large gate loops (transistor's source side)
$MN1_{off}$	V	Signal in the level-down shifter circuit in the gate driver based on HVCS
$MN2_{EN}$	V	Signal in the gate driver based on HVCS
MN_{B1}		High-voltage transistor of the "V_{HV} control" circuit
MN_{B2}		High-voltage transistor of the "V_{HV} control" circuit
MN_R		Transistor for active rectification in the gate driver based on HVES
MN_n		PMOS transistor of the gate driver based on HVES (transistor's source side)
MN_p		PMOS transistor of the gate driver based on HVES (transistor's gate side)
MN_n		NMOS transistor of the gate driver based on HVES (transistor's source side)
MN_p		NMOS transistor of the gate driver based on HVES (transistor's gate side)
ω_o	1/s	Resonance frequency of the HVES circuit
R_{Bn}	Ω	Resistor of the gate driver for large gate loops based on HVES (transistor's source side)
R_{Bp}	Ω	Resistor of the gate driver for large gate loops based on HVES (transistor's gate side)
$R_{DS,on}$	Ω	Transistor on-state resistance
R_G	Ω	Gate resistor
$R_{G,on}$	Ω	Turn-on gate resistor
$R_{G,off}$	Ω	Turn-off gate resistor
R_{loop}	Ω	Gate loop resistance
R_{par}	Ω	Parasitic gate loop resistance
S	V	Source potential of the power transistor