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ICMC 2020

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Message from General Co-chairs

It gives me a great pleasure to welcome you to ICMC 2020, the 6th edition of the premier annual conference on Mathematics and Computing. This year, ICMC will be held in the Department of Computer Applications, Sikkim University, Gangtok, Sikkim, India, where advanced technology infrastructure and collection of creative talents are gathered, making it an excellent position to develop advanced Computing. ICMC has been the most impactful conference on all aspects of Mathematics and Computing. Papers published in this impactful conference represent the hard work of many outstanding researchers from around the world. We are very delighted to report that ICMC remains at the forefront of computer networks. This year, the main conference embodies a set of 45 papers out of 172 submissions, selected through careful and rigorous peer review by TPC members as best of the best submissions, and organized around 2 tracks and 18 keynote sessions. It is our honour to have invited most prominent scholars as our conference: Prof. Dipanwita Roy Chowdhury, IIT Kharagpur, India; Prof. P. D. Srivastava, IIT Bhilai, India; Dr. P. K. Saxena, DRDO, India; Prof. S. Ponnusamy, IIT Madras, India; Prof. Samiran Chattopadhyay, Jadavpur University, India; Dr. Ashok Kumar Das, IIIT Hyderabad; Dr. Sanasam Ranbir Singh, IIT Guwahati, India; Dr. Biswapati Jana, Vidyasagar University, India; Prof. Ekrem SAVAS, Usak University, Usak/Turkey; Mr. Aninda Bose, Springer, India; Prof. Duan Li, City University of Hong Kong, Hong Kong; Prof. Bidyut B. Chaudhuri, Techno India University, Kolkata, and ISI Kolkata, India; Prof. Neeraj Kumar, Thapar Institute of Engineering and Technology, India; Mr. Giovanni BluMitolo, Italy; Dr. Bidyut Kr. Patra, NIT Rourkela, Dr. Debasis Giri, MAKAUT, WB, India; Prof. Debashis De, MAKAUT, WB, India; and Dr. Swadesh Kumar Sahoo, Indian Institute of Technology Indore, India.

First, we would like to thank to all program members and organizing committee members who have done an outstanding job in carrying out the paper review tasks. In particular, we would like to express our appreciation to Dr. Debasis Giri and Mr. Partha Pratim Ray who spent great effort to develop the review system. We would like to thank Honourable Vice-Chancellor of Sikkim University, Sikkim, for his support for providing Excellent Venue. Last but not least, we thank our patrons

and sponsors for their warm support. We must thank IEEE Fellow Prof. Rajkumar Buyya for his tireless effort and constant support of ICMC 2020 for his guidance and direction.

Finally, we thank all the conference participants for making ICMC a success.

P. K. Saxena
P. D. Srivastava
Debashis De

Message from Program Co-chairs

It is a great pleasure for us to organize the Sixth International Conference on Mathematics and Computing 2020 held from March 18–20, 2020, at Gangtok, Sikkim, India. Our main goal is to provide an opportunity to the participants to learn about contemporary research in Mathematics and Computing, and exchange ideas among themselves and with experts present in the conference as tutorial presenters and the plenary as well as invited speakers.

Sixteen speakers from India and abroad agreed to deliver their talks and some of them acted as session chairs. After an initial call for papers, 172 papers were submitted at the conference. All submitted papers were sent to external referees and, after refereeing, 45 papers were recommended for publication for the conference proceedings that will be published by Springer series: *Advances in Intelligent Systems and Computing*.

ICMC 2020 has come up as an international platform to deliver and share novel knowledge in various fields on applied mathematics and computing of interest.

We are grateful to the chief patron, patron, general co-chairs, program co-chairs, publicity chair, speakers, participants, referees, organizers, sponsors, and funding agencies for their support and help without which it would have been impossible to organize the conference. We owe our gratitude to the volunteers who work behind the scene tirelessly in taking care of the details in making this conference a success.

Debasis Giri
S. Ponnusamy
Satish Narayana Srirama
Jemal Hussien
Andrew Adamatzky

Preface

In the last two decades, scientific computing has become an important contributor to all scientific research programs. It is particularly important for the solution of research problems that are unsolvable by traditional theory and experimental approaches, hazardous to study in the laboratory, or time-consuming or expensive to be solved by traditional means. With mathematical modeling and computational algorithms, many more problems from the realm of science, commerce as well as other walks of life can be solved efficiently. The International Conference on Mathematics and Computing (ICMC) is such a premier forum for the presentation of new advances and research results in the fields of Cryptography, Network Security, Cybersecurity, Internet of Things, Edge Computing, Mathematics, Statistics and Scientific Computing. The conference will bring together leading academic scientists, experts from industry, and researchers in their domains of expertise from around the world. Earlier, ICMC was organized in 2013, 2015, 2017, 2018, and 2019.

The 6th ICMC 2020 aims to bring together both novice and experienced scientists with developers, to meet new colleagues, collect new ideas, and establish new cooperation between research groups and provide a platform for researchers from academic and industry to present their original work and exchange ideas, information, techniques, and applications in the field of Computational Applied Mathematics, including, but not limited to the broad topics of Operations Research, Soft Computing, Cryptology, Network Security, Cybersecurity, Internet of Things, Edge Computing, Image Processing, Pure and Applied Mathematics, and other emerging areas of research.

The 6th ICMC 2020 is organized by the Department of Computer Applications, Sikkim University, Gangtok, Sikkim, India. This conference received 172 papers from different parts of India as well as world. This book of abstracts contains 45 full papers which fall under mathematics and computing tracks. We would like to thank the Vice-Chancellor and officials of Sikkim University, patron, respected general co-chairs, publicity chair, organizing committee members, volunteers, sponsors,

attendees, and authors who attended and made this conference a success. ICMC 2020 proceedings will be published in the Springer series: Advances in Intelligent Systems and Computing.

Haringhata, India
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Haringhata, India
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Geelong, Australia

Debasis Giri
Rajkumar Buyya
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Debashis De
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About the Editors

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Preventing Differential Fault Analysis Attack on AEGIS Family of Ciphers



Swapan Maiti and Dipanwita Roy Chowdhury

Abstract AEGIS, a dedicated authenticated encryption algorithm is one of the winners of the CAESAR portfolio. In literature, there exist fault attacks on AEGIS family of ciphers. Fault attack is one of the most efficient forms of side-channel attacks against implementations of cryptographic algorithms, and the protection against fault attack is vital for security-related devices. In this paper, we propose countermeasures for AEGIS family of ciphers. The proposed countermeasures show that the state of the ciphers can not be recovered faster than exhaustive search because it needs 2^{128} time to recover a state of each cipher.

Keywords Authenticated encryption · Fault attack · Countermeasures · CAESAR · AES

1 Introduction

Authenticated encryption (AE) and authenticated encryption with associated data (AEAD) are forms of encryption which simultaneously assure the confidentiality and authenticity of data. CAESAR [1], a competition for authenticated encryption was started in 2013, which targets to identify a portfolio of AEAD. AEGIS [2], a dedicated AES [3]-based authenticated encryption algorithm is a one of the winners of the CAESAR competition.

Fault attack is one of the most efficient forms of side-channel attack against implementations of cryptographic algorithms. In this kind of attack, faults are injected during cipher operations. The attacker then analyzes the fault-free and faulty ciphertexts or keystreams to deduce partial or full information of the secret key.

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In literature, there exist some fault attacks on authenticated encryption stream ciphers and the countermeasures [4–6]. AEGIS is also susceptible to Differential Fault Attack (DFA) [7].

The main contribution of this work can be summarized below:

- Proposed countermeasures against differential fault attack for each of the ciphers of AEGIS family.
- Furnished a comparison of the modified AEGIS with AEGIS family

The organization of the rest of the paper is as follows. Section 2 discusses AEGIS family of ciphers. The differential fault analysis on each of the ciphers is briefly described in this section. Section 3 presents the countermeasures against fault attack on each of the ciphers. A comparison of the modified AEGIS with AEGIS family is shown in Sect. 4. Finally, the paper is concluded in Sect. 5.

2 Background

The authenticated encryption algorithms of AEGIS family of ciphers are introduced in [2]. In this section, we briefly describe the ciphers and the attack strategies on them. The AEGIS family of ciphers extensively uses one keyed round function (*AESRoundFunction*) of AES [3] as follows:

$$AESRoundFunction(A, B) = \tau(A) \oplus B$$

where $\tau(\cdot) = \text{MixColumns}(\text{ShiftRows}(\text{SubBytes}(\cdot)))$, and each of A and B is a 16-byte block. The following operators are used in AEGIS:

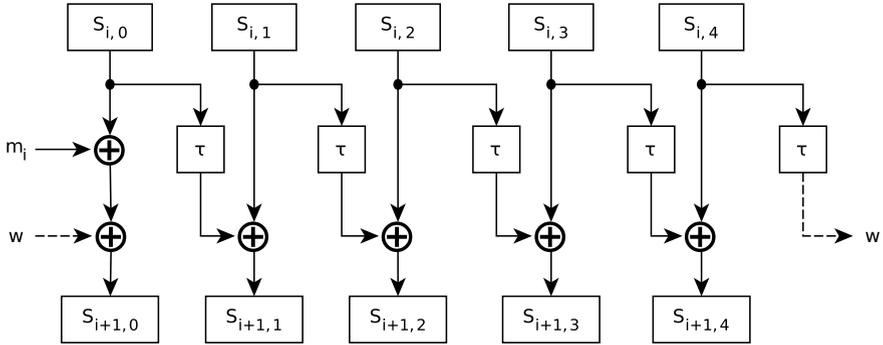
- \oplus : bit-wise exclusive OR
- $\&$: bit-wise AND
- \parallel : concatenation

2.1 AEGIS Family of Ciphers

In this section, we briefly describe the ciphers AEGIS-128, AEGIS-256, and AEGIS-128L. The ciphertext and tag generation for each cipher of AEGIS family are done in four phases: (1) The initialization, (2) Processing the associated data, (3) The encryption, and (4) The finalization. Each of the ciphers takes a 128-bit key and a 128-bit nonce.

AEGIS-128 The 80-byte state S_i of AEGIS-128 at round i can be defined as

$$S_i = S_{i,0} \parallel S_{i,1} \parallel S_{i,2} \parallel S_{i,3} \parallel S_{i,4}$$



τ : AES encryption round function without XORing with the round key
 m_i : a 16-byte data block in the round i
 w : a temporary 16-byte word

Fig. 1 The state update function of AEGIS-128

where each $S_{i,j}$, $j = 0$ to 4 , is a 16-byte block. At each round i , a 16-byte data block m_i is used to update the state S_i . The next state S_{i+1} is computed as follows:

$$\begin{aligned} S_{i+1,0} &= AESRoundFunction(S_{i,4}, S_{i,0} \oplus m_i) \\ S_{i+1,1} &= AESRoundFunction(S_{i,0}, S_{i,1}) \\ S_{i+1,2} &= AESRoundFunction(S_{i,1}, S_{i,2}) \\ S_{i+1,3} &= AESRoundFunction(S_{i,2}, S_{i,3}) \\ S_{i+1,4} &= AESRoundFunction(S_{i,3}, S_{i,4}) \end{aligned}$$

The state update function is shown in Fig. 1. In the encryption (i.e., third phase), a 16-byte plaintext P_i at round i is used to update the state, and P_i is encrypted to a 16-byte ciphertext C_i as $C_i = P_i \oplus Z_i$, where $Z_i = S_{i,1} \oplus S_{i,4} \oplus (S_{i,2} \& S_{i,3})$ is a 16-byte keystream block.

AEGIS-256 The 96-byte state S_i of AEGIS-256 at round i can be defined as

$$S_i = S_{i,0} || S_{i,1} || S_{i,2} || S_{i,3} || S_{i,4} || S_{i,5}$$

where each $S_{i,j}$, $j = 0$ to 5 , is a 16-byte block. At each round i , a 16-byte data block m_i is used to update the state S_i . The next state S_{i+1} is computed as follows:

$$\begin{aligned}
S_{i+1,0} &= AESRoundFunction(S_{i,5}, S_{i,0} \oplus m_i) \\
S_{i+1,1} &= AESRoundFunction(S_{i,0}, S_{i,1}) \\
S_{i+1,2} &= AESRoundFunction(S_{i,1}, S_{i,2}) \\
S_{i+1,3} &= AESRoundFunction(S_{i,2}, S_{i,3}) \\
S_{i+1,4} &= AESRoundFunction(S_{i,3}, S_{i,4}) \\
S_{i+1,5} &= AESRoundFunction(S_{i,4}, S_{i,5})
\end{aligned}$$

In the encryption (i.e., third phase), a 16-byte plaintext P_i at round i is used to update the state, and P_i is encrypted to a 16-byte ciphertext C_i as $C_i = P_i \oplus Z_i$, where $Z_i = S_{i,1} \oplus S_{i,4} \oplus S_{i,5} \oplus (S_{i,2} \& S_{i,3})$ is a 16-byte keystream block.

AEGIS-128L The 128-byte state S_i of AEGIS-128L at round i can be defined as

$$S_i = S_{i,0} || S_{i,1} || S_{i,2} || S_{i,3} || S_{i,4} || S_{i,5} || S_{i,6} || S_{i,7}$$

where each $S_{i,j}$, $j = 0$ to 7 , is a 16-byte block. At each round i , two 16-byte data blocks m_{2i} and m_{2i+1} are used to update the state S_i . The next state S_{i+1} is computed as follows:

$$\begin{aligned}
S_{i+1,0} &= AESRoundFunction(S_{i,7}, S_{i,0} \oplus m_{2i}) \\
S_{i+1,1} &= AESRoundFunction(S_{i,0}, S_{i,1}) \\
S_{i+1,2} &= AESRoundFunction(S_{i,1}, S_{i,2}) \\
S_{i+1,3} &= AESRoundFunction(S_{i,2}, S_{i,3}) \\
S_{i+1,4} &= AESRoundFunction(S_{i,3}, S_{i,4} \oplus m_{2i+1}) \\
S_{i+1,5} &= AESRoundFunction(S_{i,4}, S_{i,5}) \\
S_{i+1,6} &= AESRoundFunction(S_{i,5}, S_{i,6}) \\
S_{i+1,7} &= AESRoundFunction(S_{i,6}, S_{i,7})
\end{aligned}$$

In the encryption phase, two 16-byte plaintext P_{2i} and P_{2i+1} at round i are used to update the state, and P_{2i} and P_{2i+1} are encrypted to two 16-byte ciphertext C_{2i} as $C_{2i} = P_{2i} \oplus Z_{2i}$ and C_{2i+1} as $C_{2i+1} = P_{2i+1} \oplus Z_{2i+1}$, respectively, where $Z_{2i} = S_{i,1} \oplus S_{i,6} \oplus (S_{i,2} \& S_{i,3})$ and $Z_{2i+1} = S_{i,2} \oplus S_{i,5} \oplus (S_{i,6} \& S_{i,7})$ are two 16-byte keystream blocks.

2.2 Attack Description for AEGIS Family

Differential Fault Analysis of AEGIS family of ciphers is introduced in [7]. One can find a state of the ciphers by DFA, and eventually, mount forgery attack [8] by the change of one ciphertext and the associated authentication tag. Here, we present the attack description in detail.

2.2.1 Attack Model

The attacker can run the cipher with the same secret key, public parameters, and plaintext several times. The attacker is able to inject single-bit faults. The attacker has control on the timing of fault injection, and on the fault location. The plaintext and the corresponding fault-free/faulty ciphertext are available to the attacker.

Attack on AEGIS-128 The states of the cipher at rounds i and $i + 1$ are as follows:

$$S_i = S_{i,0} || S_{i,1} || S_{i,2} || S_{i,3} || S_{i,4}$$

$$S_{i+1} = S_{i+1,0} || S_{i+1,1} || S_{i+1,2} || S_{i+1,3} || S_{i+1,4}$$

By the encryption, the generated ciphertext C_i at round i , C_{i+1} at round $i + 1$ are given by $C_i = P_i \oplus Z_i$ and $C_{i+1} = P_{i+1} \oplus Z_{i+1}$, respectively, where

$$Z_i = S_{i,1} \oplus S_{i,4} \oplus (S_{i,2} \& S_{i,3}) \quad (1)$$

$$Z_{i+1} = S_{i+1,1} \oplus S_{i+1,4} \oplus (S_{i+1,2} \& S_{i+1,3}) \quad (2)$$

The state $S_i = S_{i,0} || S_{i,1} || S_{i,2} || S_{i,3} || S_{i,4}$ can be recovered by injecting 3×128 single-bit faults. The state recovery procedure is illustrated in Table 1.

Attack on AEGIS-256 Let the states of the cipher at rounds i , $i + 1$, and $i + 2$ be S_i , S_{i+1} , and S_{i+2} , respectively. By the encryption, the generated ciphertext C_i at round i , C_{i+1} at round $i + 1$, and C_{i+2} at round $i + 2$ are given by $C_i = P_i \oplus Z_i$, $C_{i+1} = P_{i+1} \oplus Z_{i+1}$, and $C_{i+2} = P_{i+2} \oplus Z_{i+2}$, respectively, where

Table 1 Recovering the cipher state of AEGIS-128

Steps	Blocks recovered	Recovering procedure
1	$S_{i,2}$	Injecting 128 single-bit faults into $S_{i,3}$ block, and using faulty Z_i and fault-free Z_i by Eq. (1)
2	$S_{i,3}$	Injecting 128 single-bit faults into $S_{i,2}$ block, and using faulty Z_i and fault-free Z_i by Eq. (1)
3	$S_{i+1,2}$	Injecting 128 single-bit faults into $S_{i+1,3}$ block, and using faulty Z_{i+1} and fault-free Z_{i+1} by Eq. (2)
4	$S_{i,1}$	Using $S_{i+1,2} = AESRoundFunction(S_{i,1}, S_{i,2}) = \tau(S_{i,1}) \oplus S_{i,2}$ by the inverse round function
5	$S_{i,4}$	Using Eq. (1)
6	$S_{i+1,3}$	Using $S_{i+1,3} = AESRoundFunction(S_{i,2}, S_{i,3}) = \tau(S_{i,2}) \oplus S_{i,3}$
7	$S_{i+1,4}$	Using $S_{i+1,4} = AESRoundFunction(S_{i,3}, S_{i,4}) = \tau(S_{i,3}) \oplus S_{i,4}$
8	$S_{i+1,1}$	Using Eq. (2)
9	$S_{i,0}$	Using $S_{i+1,1} = AESRoundFunction(S_{i,0}, S_{i,1}) = \tau(S_{i,0}) \oplus S_{i,1}$ by the inverse round function

Table 2 Recovering the cipher state of AEGIS-256

Steps	Blocks recovered	Recovering procedure
1	$S_{i,2}$	Injecting 128 single-bit faults into $S_{i,3}$ block, and using faulty Z_i and fault-free Z_i by Eq. (3)
2	$S_{i,3}$	Injecting 128 single-bit faults into $S_{i,2}$ block, and using faulty Z_i and fault-free Z_i by Eq. (3)
3	$S_{i+1,2}$	Injecting 128 single-bit faults into $S_{i+1,3}$ block, and using faulty Z_{i+1} and fault-free Z_{i+1} by Eq. (4)
4	$S_{i+1,3}$	Using $S_{i+1,3} = AESRoundFunction(S_{i,2}, S_{i,3}) = \tau(S_{i,2}) \oplus S_{i,3}$
5	$S_{i,1}$	Using $S_{i+1,2} = AESRoundFunction(S_{i,1}, S_{i,2}) = \tau(S_{i,1}) \oplus S_{i,2}$ by the inverse round function
6	$S_{i+2,3}$	Using $S_{i+2,3} = AESRoundFunction(S_{i+1,2}, S_{i+1,3}) = \tau(S_{i+1,2}) \oplus S_{i+1,3}$
7	$S_{i+2,2}$	Injecting 128 single-bit faults into $S_{i+2,3}$ block, and using faulty Z_{i+2} and fault-free Z_{i+2} by Eq. (5)
8	$S_{i+1,1}$	Using $S_{i+2,2} = AESRoundFunction(S_{i+1,1}, S_{i+1,2}) = \tau(S_{i+1,1}) \oplus S_{i+1,2}$ by the inverse round function
9	$S_{i,0}$	Using $S_{i+1,1} = AESRoundFunction(S_{i,0}, S_{i,1}) = \tau(S_{i,0}) \oplus S_{i,1}$ by the inverse round function
10	$(S_{i,4} \oplus S_{i,5})$	Using Eq. (3)
11	$S_{i,4}$	Using Eq. (4) defined as $Z_{i+1} = S_{i+1,1} \oplus \tau(S_{i,3}) \oplus S_{i,4} \oplus \tau(S_{i,4}) \oplus S_{i,5} \oplus (S_{i+1,2} \& S_{i+1,3})$
12	$S_{i,5}$	From known $(S_{i,4} \oplus S_{i,5})$ and $S_{i,4}$

$$Z_i = S_{i,1} \oplus S_{i,4} \oplus S_{i,5} \oplus (S_{i,2} \& S_{i,3}) \quad (3)$$

$$Z_{i+1} = S_{i+1,1} \oplus S_{i+1,4} \oplus S_{i+1,5} \oplus (S_{i+1,2} \& S_{i+1,3}) \quad (4)$$

$$Z_{i+2} = S_{i+2,1} \oplus S_{i+2,4} \oplus S_{i+2,5} \oplus (S_{i+2,2} \& S_{i+2,3}) \quad (5)$$

The state $S_i = S_{i,0} || S_{i,1} || S_{i,2} || S_{i,3} || S_{i,4} || S_{i,5}$ can be recovered by 4×128 single-bit faults. The state recovery procedure is illustrated in Table 2.

Attack on AEGIS-128L Let the states of the cipher at rounds i and $i + 1$ be S_i and S_{i+1} , respectively. By the encryption, the generated ciphertext C_{2i} and C_{2i+1} at round i , C_{2i+2} and C_{2i+3} at round $i + 1$ are given by $C_{2i} = P_{2i} \oplus Z_{2i}$, $C_{2i+1} = P_{2i+1} \oplus Z_{2i+1}$, $C_{2i+2} = P_{2i+2} \oplus Z_{2i+2}$, and $C_{2i+3} = P_{2i+3} \oplus Z_{2i+3}$, respectively, where

$$Z_{2i} = S_{i,1} \oplus S_{i,6} \oplus (S_{i,2} \& S_{i,3}) \quad (6)$$

$$Z_{2i+1} = S_{i,2} \oplus S_{i,5} \oplus (S_{i,6} \& S_{i,7}) \quad (7)$$

$$Z_{2i+2} = S_{i+1,1} \oplus S_{i+1,6} \oplus (S_{i+1,2} \& S_{i+1,3}) \quad (8)$$

$$Z_{2i+3} = S_{i+1,2} \oplus S_{i+1,5} \oplus (S_{i+1,6} \& S_{i+1,7}) \quad (9)$$

Table 3 Recovering the cipher state of AEGIS-128L

Steps	Blocks recovered	Recovering procedure
1	$S_{i,2}$	Injecting 128 single-bit faults into $S_{i,3}$ block, and using faulty Z_{2i} and fault-free Z_{2i} by Eq. (6)
2	$S_{i,3}$	Injecting 128 single-bit faults into $S_{i,2}$ block, and using faulty Z_{2i} and fault-free Z_{2i} by Eq. (6)
3	$S_{i,6}$	Injecting 128 single-bit faults into $S_{i,7}$ block, and using faulty Z_{2i+1} and fault-free Z_{2i+1} by Eq. (7)
4	$S_{i,7}$	Injecting 128 single-bit faults into $S_{i,6}$ block, and using faulty Z_{2i+1} and fault-free Z_{2i+1} by Eq. (7)
5	$S_{i,1}$	Using Eq. (6)
6	$S_{i,5}$	Using Eq. (7)
7	$S_{i+1,2}$	Using $S_{i+1,2} = AESRoundFunction(S_{i,1}, S_{i,2}) = \tau(S_{i,1}) \oplus S_{i,2}$
8	$S_{i+1,3}$	Using $S_{i+1,3} = AESRoundFunction(S_{i,2}, S_{i,3}) = \tau(S_{i,2}) \oplus S_{i,3}$
9	$S_{i+1,6}$	Using $S_{i+1,6} = AESRoundFunction(S_{i,5}, S_{i,6}) = \tau(S_{i,5}) \oplus S_{i,6}$
10	$S_{i+1,7}$	Using $S_{i+1,7} = AESRoundFunction(S_{i,6}, S_{i,7}) = \tau(S_{i,6}) \oplus S_{i,7}$
11	$S_{i+1,1}$	Using Eq. (8)
12	$S_{i+1,5}$	Using Eq. (9)
13	$S_{i,0}$	Using $S_{i+1,1} = AESRoundFunction(S_{i,0}, S_{i,1}) = \tau(S_{i,0}) \oplus S_{i,1}$ by the inverse round function
14	$S_{i,4}$	Using $S_{i+1,5} = AESRoundFunction(S_{i,4}, S_{i,5}) = \tau(S_{i,4}) \oplus S_{i,5}$ by the inverse round function

The state $S_i = S_{i,0}||S_{i,1}||S_{i,2}||S_{i,3}||S_{i,4}||S_{i,5}||S_{i,6}||S_{i,7}$ can be recovered by 4×128 single-bit faults. The state recovery procedure is illustrated in Table 3.

3 Countermeasures

Here, we propose the countermeasures against differential fault attack on AEGIS family by slight modification of the 16-byte block keystream generation in the encryption function. By the modified encryption functions, one can not recover a state of the ciphers of AEGIS family, and hence can not mount a forgery attack on the tag generation.

3.1 Countermeasure for AEGIS-128

We modify the keystream generation function. Under this modification, the keystreams at rounds i and $i + 1$ are as follows: