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Om Hari Gupta
Vijay Kumar Sood *Editors*

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Preface

The Electric Power and Renewable Energy Conference (EPREC-2020), organized by the Department of Electrical Engineering, National Institute of Technology Jamshedpur, India, during May 29 to 30, 2020, has been a unique conference during the difficult times of a global pandemic necessitating the usage of online presentations. We thank all the contributors for maintaining the high standard and making EPREC-2020 a huge success. Out of total 351 valid submissions, only 142 were selected for publication in three different volumes, i.e., an acceptance rate of nearly 40%. The conference attracted an international audience from the following countries: Bangladesh, Brazil, Canada, China, India, Norway, Qatar, Slovakia, Thailand, Ukraine, and USA. This volume, i.e., Recent Advances in Power System, is one of three volumes published by Springer in the book series "Lecture Notes in Electrical Engineering (LNEE)." It contains 49 high-quality papers which provide an overview of recent developments in modern power systems.

We thank all the organizing committee members, technical program committee members, reviewers, and student volunteers for their valuable support and volunteer work. We also appreciate the role of session chairs/co-chairs. We also thank the series editors of LNEE and Ms. Priya Vyas and Dr. Akash Chakraborty, Associate Editors—Applied Sciences and Engineering, Springer, for their help and quick responses during the preparation of the volume.

The editors hope that this volume will provide the readers relevant information on the latest trends in renewable energy, microgrid/smart grid operation, control, protection, HVDC systems, power system protection, etc.

Jamshedpur, India — Om Hari Gupta
Oshawa, Canada — Vijay Kumar Sood

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Om Hari Gupta is currently an Assistant Professor at the Department of Electrical Engineering, National Institute of Technology Jamshedpur, India. He received the B.Tech degree (Electrical & Electronics Engineering) from UP Technical University, Lucknow, India, M.Tech degree (Power Electronics & ASIC Design) from the MN National Institute of Technology Allahabad, Prayagraj, India, and Ph.D. degree (Electrical Engineering) from the Indian Institute of Technology Roorkee, Roorkee, India. He is a recipient of the Canadian Queen Elizabeth II Diamond Jubilee Scholarship for research visiting the University of Ontario Institute of Technology, Oshawa, ON, Canada in 2017. His major areas of research interests include power system compensation and protection, microgrid control and protection, and control of drives. Dr. Gupta is a reviewer for various international journals including IEEE Transactions on Power Delivery, Electric Power Components and Systems, International Journal of Electrical Power and Energy Systems, etc.

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Ground Fault Detection Using Pole Differential Current Measurement for 2-Terminal Bipolar HVDC Lines

Ravi Shankar Tiwari, Om Hari Gupta, and Vijay K. Sood

1 Introduction

Long-distance bulk power transmission is one of the essentials in today's electricity grids. Extra high-voltage alternating current (HVAC) transmission lines are traditionally being used for long-distance and bulk power transmission. However, high-voltage direct current (HVDC) transmission system is also gaining in popularity over existing HVAC transmission system. Some typical recent examples are the 2375 km, Rio Madeira link in Brazil, 1750 km, ±800 kV, Bishwanath–Agra corridor, in India and many more. The reasons for HVDC transmission popularity are its ability for bulk power transmission over long distances, fast and precise control of power due to asynchronous interconnection, increased line-loading (close to the thermal limit), nearly zero reactive power loss, high efficiency, cost-effectiveness, etc [1]. To ensure the smooth and reliable power flow, fast and effective transmission protection schemes are required.

Protecting HVDC lines needs a different approach as compared to HVAC lines. The HVDC line protection requires detection and interruption of DC short-circuit currents. Interrupting a DC short-circuit current is much more complex in HVDC lines as compared to HVAC lines because of the absence of natural current zero crossings and quick increase of short-circuit current to an unacceptable value. However, the

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HVDC converter control technologies provide options for clearing the fault beyond the notable approach of employing circuit breakers in the AC system [2].

Therefore, the function of HVDC line protection is to detect the DC line faults and force DC line current to zero by means of rapid control actions so as to clear the fault and restore the normal system operation as quickly as possible. Most of the faults in DC lines are temporary in nature [3] and get cleared within a short time duration. If the DC fault is permanent in nature, then converter controls are unable to extinguish the fault arc and AC breakers are used to interrupt the DC system.

Some characteristics of DC line faults are noteworthy. The magnitudes of DC fault current in HVDC systems are much lower (typically, 2–3 P.U.) when compared to AC systems. Also, a sharp voltage dip during DC line faults results in a sudden drop in DC power transmission causing huge disturbances in the attached AC systems [4, 5]. This speaks to the need and significance of rapid fault detection, clearing and system recovery.

The major challenges are to achieve the desired speed, sensitivity and reliability to clear the fault within few AC cycles. This depends on accurate real-time voltage and current measurements and high-speed communication to transfer the crucial decision-making information from one station to other. Giant magneto resistance (GMR) and Hall effect sensors based on magnetic field can be used for accurate current measurements. The GMR and Hall current sensors have a high sensitivity and dynamic range of the value of 10 mT (10 mA–35 kA) and 0.001 mT (1 mA–10 kA), respectively [6]. The principle used to implement the protection algorithm can be based on local measurement or measurement via communication at distinct locations on the DC lines [7].

In the literature, the commonly available algorithms utilize traveling wave [8], current derivative [3], differential [3] and voltage level and voltage derivative protections [9]. These protection algorithms are discussed next.

1.1 Voltage Derivative Protection [8]

The decrease in voltage and increase in current of DC line use the concept of traveling waves and calculate the derivates of measured voltage $\frac{\partial V}{\partial t}$ and current $\frac{\partial I}{\partial t}$ waves to construct the criteria for detecting faults. The polarity of the current derivative indicated whether the fault is internal or external. The weighted sum of these derivatives ($k = k_1 \frac{\partial I}{\partial t} + k_2 \frac{\partial V}{\partial t}$) is compared with a set threshold, and if found to be greater than the said threshold, a DC line fault is detected. Both the poles are required to be equipped with this function and can detect the fault within 2–3 ms. However, the technique is unable to detect remote-end faults as well as faults with high resistance because of its impedance dependency [8].

1.2 Traveling Wave (TW) Protection [8]

Traveling waves are the high-frequency transient current/voltage waves generated in the event of DC line faults and tend to move from fault point to the ends of line [8]. The protection algorithm detects the wave front of generated traveling wave from instantaneous current and voltage samples. A number of consecutive sample differences are measured and compared with a threshold value to check whether the wave has enough magnitude for a certain time period. If all the measured difference crosses the threshold, it indicates the presence of a line fault. However, the detection of wave front gets affected in long lines and large impedance faults and it is difficult to detect double-pole faults [10].

1.3 Current Differential Protection [3, 11]

In this algorithm, differential current calculated by measurement at the two ends of the DC line is compared with a threshold. If the differential current exceeds the threshold, this information is relayed to converter stations and protection is initiated. The sensitivity of this gets affected by charging and discharging currents produced due to voltage variations, especially in cables. Moreover, line current information needs to be transferred to other stations, which adds a delay, and may affect the response of the scheme. The reliability indirectly depends on reliability of telecommunication method used [3, 11].

1.4 Distance Protection [10, 12]

The distance protection scheme is widely used for AC lines. The authors of [12] suggested time-domain distance protection scheme based on distributed line model. In [10], a distance protection criterion is proposed which is based on linear distribution of low-frequency voltage signal along the line. If the polarity of low-frequency filtered voltage is opposite to the compensating voltage, it indicates the presence of an internal fault.

1.5 DC Voltage-Level Protection [3]

This method detects high impedance faults near the inverter end by measuring a dip in voltage over a large time. The time and level delays are kept so as not to cause mal-operation during normal switching or voltage transients. This method is also used as backup for traveling wave and voltage derivative schemes [3].

1.6 *Protection Based on Signal Processing Techniques [13–15]*

The use of signal processing techniques such as wavelets, artificial neural networks (ANNs) and support vector machines (SVMs) has also increased as a powerful tool for AC as well as DC line protection. The authors of [13] propose a complete fault detection, localization and classification algorithm based on SVM for HVDC lines. In [14], ANN architecture is used to accurately locate the fault using AC rms voltage, DC voltage and line currents at rectifier end. A wavelet multi-resolution signal decomposition algorithm [15] is used to calculate traveling wave transient voltage energy distribution to identify the short circuit and lightning fault in HVDC line [15].

Now, to address the aforementioned issues—mainly the problem of delay in protection due to involvement of data exchange and communication—this paper proposes a local fault detection criteria (independent of information from remote station) to reduce the fault detection time and improve the converter controls.

The rest of the manuscript is organized as follows. Section 2 deals with the control strategy for steady-state and dynamic operation of HVDC system. Section 3 explains proposed pole differential current algorithm for pole-to-ground fault detection, threshold criteria and its coordination with VDCO control. Section 4 presents the PSCAD/EMTDC simulation of the test system. Finally, Sect. 5 concluded the work performed.

2 HVDC Line Control Strategies

The line-commutated 6-pulse converter bridges are the basic components of the bipolar HVDC transmission system, as shown in Fig. 1. The objectives of HVDC control [1] are (a) to limit the maximum DC line current, (b) to maintain the maximum

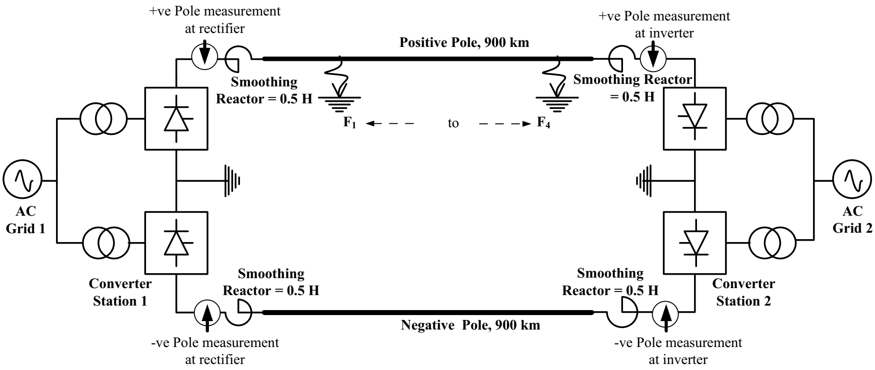


Fig. 1 2-terminal bipolar HVDC test system

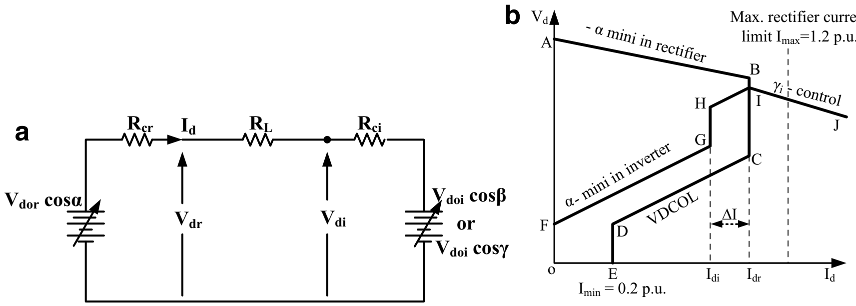


Fig. 2 **a** Steady-state equivalent circuit. **b** Controller characteristics

DC voltage for transmission and (c) to minimize reactive power consumption for steady-state and dynamic conditions of the HVDC system. The steady-state requirements are to limit the non-characteristic harmonic generation, maintaining control variable DC line current (I_d) and firing angle α to accommodate any AC network topology variations. The dynamic requirements are to minimize sudden changes in the power, current, power reversal and associated AC system frequency variations.

The control strategies implemented to fulfill the steady-state and dynamic requirements are constant current (CC), minimum firing angle at rectifier end and constant voltage control, minimum extinction angle at the inverter end. The controller functions are illustrated via DC system equivalent and controller characteristics, as shown in Fig. 2(a) and 2(b), respectively.

The converter valve voltages and line current for steady-state equivalent circuit of a 2-terminal HVDC (Fig. 2(a)) are defined as

At rectifier end

$$V_{\mathrm{dr}} = V_{\mathrm{dor}} \cos\alpha - R_{\mathrm{cr}} I_d \tag{1}$$

$V_{\mathrm{dor}} = \frac{3}{\pi}\sqrt{2} V_{\mathrm{LLr}}$, $R_{\mathrm{cr}} = \frac{3}{\pi}\omega L_{\mathrm{cr}}$,

$$I_{\mathrm{d}} = \frac{V_{\mathrm{dor}} \cos\alpha - V_{\mathrm{doi}} \cos\gamma}{R_{\mathrm{cr}} + R_{\mathrm{L}} - R_{\mathrm{ci}}} \tag{2}$$

At inverter end

$$-V_{\mathrm{di}} = V_{\mathrm{doi}} \cos\beta + R_{\mathrm{ci}} I_{\mathrm{d}} \tag{3}$$

Or

$$-V_{\mathrm{di}} = V_{\mathrm{doi}} \cos\gamma - R_{\mathrm{ci}} I_{\mathrm{d}} \tag{4}$$

$$V_{\mathrm{doi}} = \frac{3}{\pi}\sqrt{2} V_{\mathrm{LLi}} \tag{5}$$

where V_{LLr}, V_{LLi} are the AC-side line-to-line voltages at rectifier and inverter stations. R_{L} is the DC line resistance, and R_{cr}, R_{ci} are the equivalent commutation resistances of rectifier and inverter bridges. Figure 2(b) shows the modified control characteristics ABCDE and FGHIJ of rectifier and inverter stations, respectively. The details for both are described in Tables 1 and 2 to fulfill the steady-state and dynamic requirements.

Table 1 Rectifier station requirements and control implementation

Line section	Control implemented	Features obtained	Reason
AB	α-minimum	Higher loading and minimized reactive power consumption	To enhance power flow, power factor
BC	Constant current (CC) $I_{\mathrm{dr(limit)}} = 1$ P.U.	Limit maximum DC line current I_{d} (during inverter-side voltage dip rectifier operates in CC)	For valve protection
CD	Voltage-dependent current order limit (VDCOL)	Operates the HVDC link with reduced power flowing under sudden huge voltage dip	To maintain lower current margin for reduced power flow
DE	Minimum current $I_{\mathrm{min}} = 0.2$ P.U.	To avoid zero current through converter valves due to harmonics generates HV stresses	Valve protection

Table 2 Inverter station requirements and control implementation

Point on curve	Control implemented	Features obtained	Reason
IJ	γ-minimum (CEA)	Provide voltage controller at inverter, and maintain constant voltage for steady-state operation	Improved power factor during operation
HI	Constant β	Stable operation during heavy voltage dip at rectifier during week AC system interconnection	Avoided multiple operation of controller
GH	Constant current (CC)	To get an intersection point between rectifier and inverter characteristics, CC must be provided at inverter	Maintain power flow in HVDC link
FG	α-minimum	Operates the HVDC link with reduced power flowing under sudden large voltage dip	To avoid commutation failure during AC faults

The intersection point of the two characteristics shows the operating point of HVDC link.

3 Proposed Pole Differential Current Algorithm

3.1 Protection Principle

The probability of faults in the DC line is higher as compared to any other part of the HVDC system. Most of the faults in DC lines are temporary which are initiated due to pollution or lightning strikes. Pole-to-ground fault is one of the most frequently caused faults due to insulation failure between line conductor and ground [16].

The traditional current differential protection algorithm has good reliability but depends on the communication channel. To minimize the dependency on the communication channel and enhance the reliability and sensitivity, single-end measurement-based protection scheme is introduced. The proposed scheme uses a measurement at rectifier side using high-sensitivity GMR or Hall sensors. The measurement performed on both poles is shown in Fig. 1. The measured samples of instantaneous currents are used to obtain the pole differential current (PDC) as shown in (6) which is compared with the threshold, and if found greater than the said threshold, an internal fault is declared.

For normal load and external fault conditions, the PDC will be negligible. The sudden rise in differential current guaranties the presence of an internal fault, but to enhance the security; it should be compared with a set threshold. The amplitude of differential current gets affected by fault resistance and fault location. Still the scheme is sensitive enough for fault resistances up to 500 Ω.

The current measurements are performed at each station, i.e., $I_{\mathrm{PR}}(t)$, $I_{\mathrm{NR}}(t)$, $I_{\mathrm{PI}}(t)$ and $I_{\mathrm{NI}}(t)$. The PDC calculated at inverter and rectifier stations is given by

Pole differential current (PDC) at rectifier end $\Delta I_{\mathrm{Pole1}}(t)$ is given below in (6):

$$\Delta I_{\mathrm{Pole1}}(t) = (I_{\mathrm{PR}}(t) - I_{\mathrm{NR}}(t)) \tag{6}$$

Pole differential current (PDC) at inverter end $\Delta I_{\mathrm{Pole2}}(t)$ is given below in (7):

$$\Delta I_{\mathrm{Pole2}}(t) = (I_{\mathrm{PI}}(t) - I_{\mathrm{NI}}(t)) \tag{7}$$

where $\Delta I_{\mathrm{Pole1}}(t)$ and $\Delta I_{\mathrm{Pole2}}(t)$ are PDC obtained by subtracting positive and negative instantaneous current samples at both stations. The pole-to-ground fault is detected when it satisfies the criteria of (8):

$$\Delta I_{\mathrm{Pole}}(t) > I_{\mathrm{th}} \tag{8}$$

where I_{th} is the threshold for PDC. Whenever this criterion is satisfied—giving an indication of fault—the local or master controller was instructed for necessary actions.

3.2 Selection of Threshold

Since the bipolar HVDC transmission system, under normal or external fault operation, gives negligible PDC, so the selection of minimum threshold current increases the sensitivity with low fault detection time. Based on the rigorous simulation study presented in the next section, the threshold used for identifying the fault detection time is set at 0.25 P.U.

3.3 Coordination of PDC and VDCOL Control Characteristics

The normal control-based protection against DC line faults is the use of the static VDCOL characteristic. This is effective to reduce the DC fault current to a level of 0.2 P.U. as indicated in Fig. 2 and works well in most cases of a temporary DC line fault. However, in the case of a permanent DC line fault, the VDCOL characteristic is unable to extinguish the DC fault arc and reduce the DC fault current to zero. In such a case, the PDC will activate the opening of the AC-side breaker at the rectifier end to extinguish the DC fault arc after a preselected period of time.

4 Simulation Results and Discussion

A 2-terminal bipolar HVDC transmission system (Fig. 1) is simulated in PSCAD/EMTDC, and pole-to-ground faults are created at various locations, i.e., at F_1, F_2, F_3 and F_4. System data and controller details are provided in the Appendix. The measured and sampled data is exported to MATLAB software for the implementation of the protection algorithm.

For a pole-to-ground fault at location F_1 (0 km from the rectifier end) and fault resistance R_1, the DC pole currents and PDC are plotted in Fig. 3. Similarly, Fig. 4 presents the DC pole currents and PDCs for fault at F_4 (900 km) with fault resistance R_4. In both the cases, the current of the faulty pole varies largely and the current of healthy pole hardly changes. The PDCs at the rectifier and inverter ends also detect and cross the thresholds—indicating the internal pole-to-ground fault. A few cases for various fault locations F_1 to F_4 where $F_1 = 0$ km, $F_2 = 300$ km, $F_3 = 600$ km and $F_4 = 900$ km are considered with the variations in fault resistance and fault

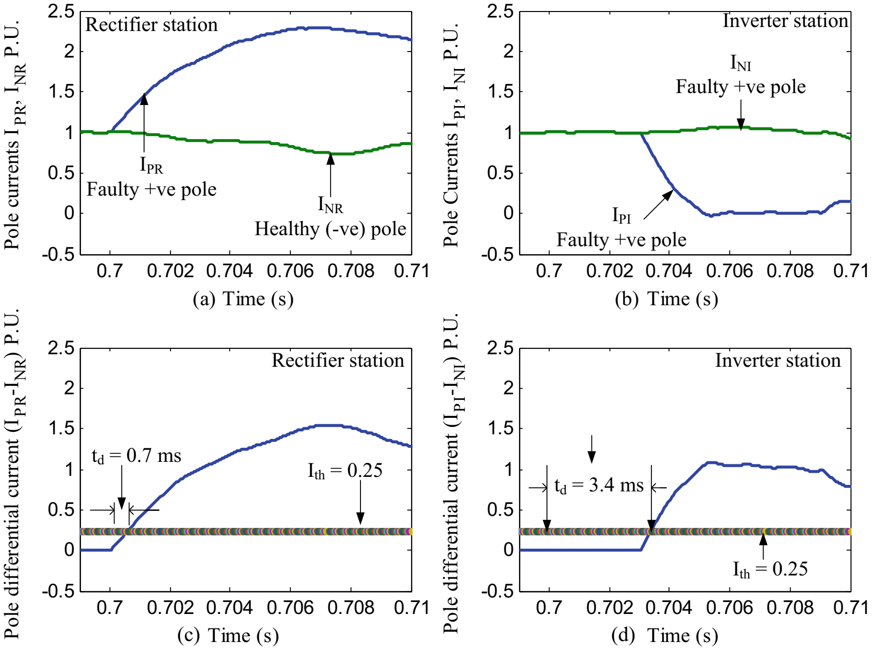


Fig. 3 DC line currents, PDCs and fault detection time (t_d) for F_1, R_1

detection time is recorded (Table 3). From the obtained results, it is found that the highest fault detection time is at 500 Ω fault resistance at location F_4 which is 5.1ms. Similar measurement and calculation are performed at inverter station also to obtain various fault detection times based on different fault locations and resistances. The results show smaller fault detection time as compared to other schemes, and thus the scheme can be preferred for primary protection against ground faults in DC lines.

Here, t_{dr} and t_{di} are the fault detection times at rectifier and inverter stations, respectively, as listed in Table 3.

The proposed PDC algorithm gives stable response during any variations in reference power through the HVDC link. Figure 5 presents the reference current, positive and negative pole currents, and PDC in response to changes in the reference loading condition from 1 to 0.5 P.U. for time duration of 1 s. Since the master control is same for both the poles, any variation in reference power is simultaneously applied to both positive and negative poles. Thus, similar variation in each DC line current to accommodate the command from master controller leads to nearly zero PDC which is desired for stable operation.

Similarly, the PDC algorithm gives stable response at inverter end also for any step variation in reference power in the HVDC link. Thus, the scheme is accurate for protection against ground fault having least detection time, good sensitivity and high reliability due to elimination of data transfer and communication delay.

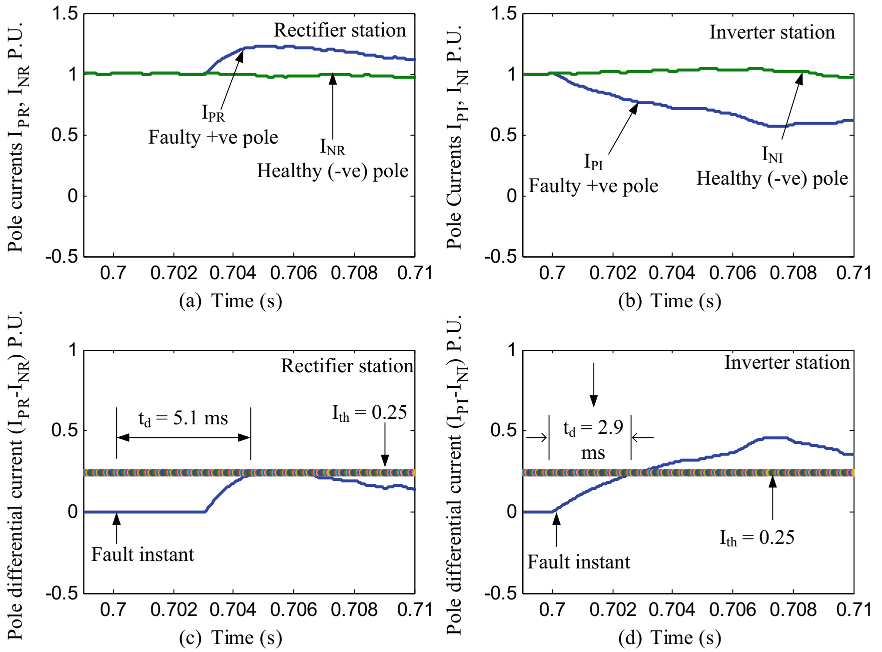


Fig. 4 DC line currents, PDCs and fault detection time (t_d) for F_4, R_4

Table 3 Fault detection time with fault location and transition resistance

Fault location	Fault detection times t_{dr}/t_{di} (ms) for threshold $I_{th} = 0.25$ P.U.				Fault detection status			
	$R_1 = 10\ \Omega$	$R_2 = 100\ \Omega$	$R_3 = 300\ \Omega$	$R_4 = 500\ \Omega$	R_1	R_2	R_3	R_4
F_1	0.7/3.4	0.9/3.6	1.6/4.0	3.1/4.8	✓	✓	✓	✓
F_2	1.4/2.4	1.7/2.7	2.5/3.5	4.7/4.3	✓	✓	✓	✓
F_3	2.4/1.3	2.7/1.7	3.6/2.5	4.4/4.0	✓	✓	✓	✓
F_4	3.5/0.7	3.6/1.0	4.1/1.8	5.1/2.9	✓	✓	✓	✓

5 Conclusion

The paper presents a thorough analysis of a 2-terminal bipolar HVDC system control and the protection algorithm against DC line faults. Importance of fast fault detection and response from these faults by control strategies are explained. Most of the available detection algorithms have delay in protection due to communication between inverter and rectifier ends for measured data transmission. The proposed algorithm is based on the calculation of pole differential currents at both ends to avoid the delay due to information exchange and therefore speeds up the protection. The HVDC

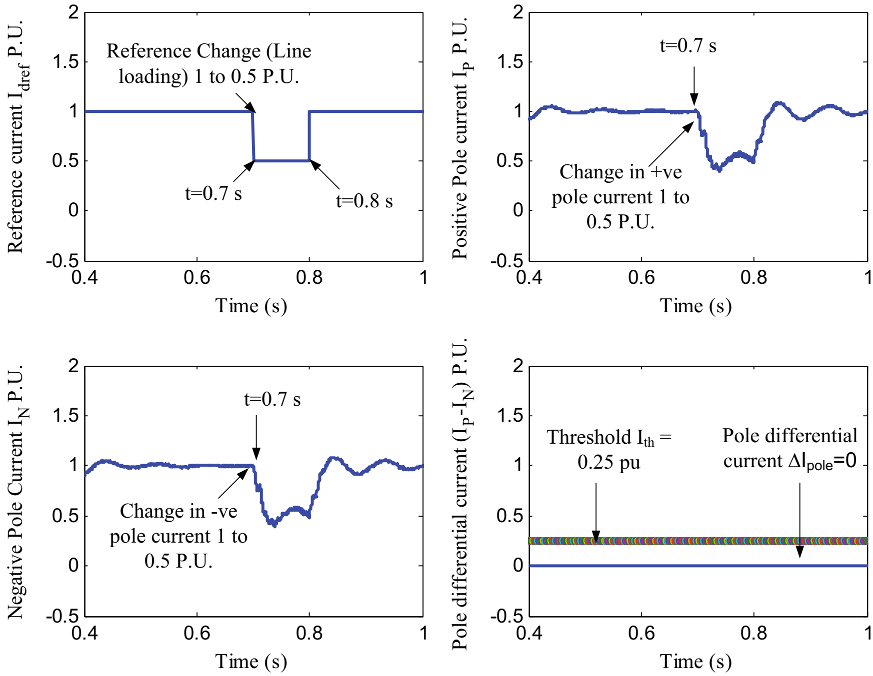


Fig. 5 PDC algorithm response during change in reference power loading at rectifier end

line faults, i.e., pole-to-ground faults, were implemented with the combination of various fault resistances and fault locations to observe the effect on fault detection. The simulated results show that the proposed PDC algorithms have the advantage of improved fault detection time and protection reliability and are useful as primary protection schemes for HVDC lines against line-to-ground short-circuit faults.

Appendix 1

Bipolar HVDC Test System

The data for the system configuration (Fig. 1) is obtained from the MATLAB model (based on a Hydro-Quebec-)mono-polar HVDC model which is modified into a bipolar HVDC system. The Hydro-Quebec system was developed for steady-state and transient analysis of a 12-pulse, 1000 MW (500 kV–2kA) 50/60 Hz HVDC transmission system. The system consists of two overhead transmission line conductors acting as forward paths for positive and negative poles and solidly grounding acting as return path. The HVDC link interconnects the two asynchronous AC grids. The sending end of the HVDC link is connected with 500 kV, 60 Hz, and receiving end

Table 4 Various parameters of converters and HVDC bipolar system

Components of HVDC system	Rating and specifications
Type of HVDC link	Bipolar solid grounded
Power rating	2000 MW (1000 MW each pole)
DC voltage level	±500 kV each pole
Current rating	2 kA of each pole
Converter	1200 MVA of each pole
AC grid 1 voltage	500 kV, 60 Hz, 500 MVA
AC grid 2 voltage	345 kV, 50 Hz, 10,000 MVA
Smoothing reactor	0.5 H at both ends
AC filter 1	1200 Mvar at 60 Hz
AC filter 2	1200 Mvar at 50 Hz

AC grid is of 345 kV, 50 Hz system. The line-commutated converter bipolar HVDC test system consists of two 6-pulse series-connected converters forming 12-pulse converter configuration which is connected to a 900 km distributed parameter line and smoothing reactors of 0.5 H at both ends. The various parameters of converter and HVDC bipolar system are shown in Table 4. The two 600 MVAr AC filters are connected in the system.

Appendix 2

Current Controller and Constant Extinction Angle Control (CEA)/γ-Control

The prime objective of HVDC system control is to obtain fast and flexible power control between rectifier and inverter stations under steady-state and transient operation. Usually, this system operates in constant power control mode where power order is decided by user. Power controller derives the current order supplied to VDCOL and current controller amplifier (CCA). The α-order generated from CCA is communicated to converter firing angle control to determine valve firing instants. The converter controls at rectifier and inverter stations are set to operate in constant current and constant voltage control modes, respectively; during any DC line faults, the controllers of both ends shift their operational modes from steady state so as to minimize the effect of fault on both AC–DC sides. The various converter control modes are current control (CC), voltage control, VDCOL, minimum alpha (CIA), gamma control (CEA), β-control modes. Figures 6, 7 and 8 present the pole control, current control and overview of control blocks of HVDC system.

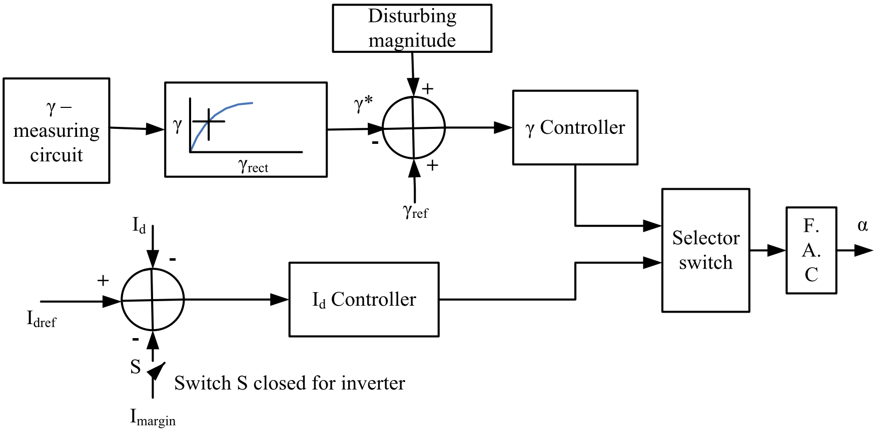
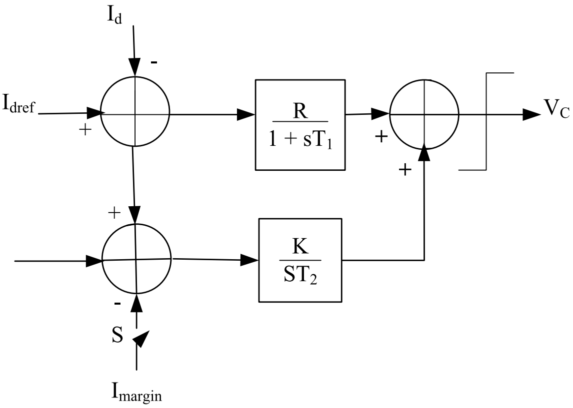


Fig. 6 Pole and converter control

Fig. 7 Current controller



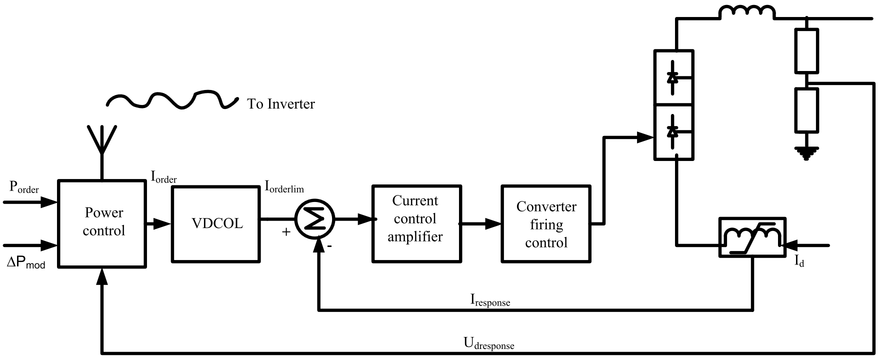


Fig. 8 HVDC control overview

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A Review on Islanding Detection Schemes for DC Microgrids

Bhabani Kumari Choudhury and Premalata Jena

1 Introduction

Recently, renewable energy sources (RESs)-based power plants have attained significant attention because of the fast depletion of fossil fuels and global warming [1]. Distributed generations (DGs), loads, and a bidirectional converter is interfaced with the utility grid in order to exchange powers [2]. DGs enhance the profit of power generation, reduce the effect of global warming, and improve power quality. Therefore, the application of DGs provides the reliability and security to the system [3, 4]. MGs are of two types, namely AC MGs and DC MGs. Operation modes of MGs can be either isolated or grid-connected modes [5]. AC MGs research is well developed because of its mature technologies, protection, and standards. Most of the DGs generate power in the form of DC, and it is converted into AC power through DC-to-AC converter (inverter) in order to connect them with the AC MGs [6]. It is important to note that DC loads need DC power supply, and hence, AC power is converted back to DC power. Here, the number of conversions, number of required converters, and losses are more, so it reduces the efficiency of the system [7]. Apart from these, stability, synchronization, and reactive power requirement are the built-in disadvantages of AC MGs. Therefore, DC MGs are a better alternative and solution to the above problems [8, 9]. Moreover, DC MGs are easily scalable because of the absence of limiting equipment, such as transformers and relays.

During islanding, utility grid connection is absent. So, DGs are the main sources at this time. But, the power can reach to the consumers without any interruption during islanding due to DGs [10]. Here, employees can be affected by islanding as

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they may not notice that some part of the circuit is working, which may stop reconnection of devices automatically [11]. In order to maintain stability, it is essential to maintain a balance between load and generation in the islanded circuit. The above-stated reasons can be avoided by rapidly detecting the islanding, so that it can be disconnected from the primary circuit as quickly as possible. This process is known as anti-islanding [12]. The requirements for IDSs in DGs are outlined in [13], which clearly indicates that DGs should disconnect from the grid within 2 s. Otherwise, it will draw a significantly high amount of current to keep the balance. Due to this, DGs are damaged.

In [14–17], some AC MGs islanding is reported. However, DC MG IDSs are in the initial stage and not rigorously studied in the literature. This paper presents an overview of islanding detection schemes, which is used for DC MGs. The requirements of DC MGs IDSs along with their advantages over the AC MGs IDSs are reported. Recent research and developments in this field are presented with possible challenges, and classification of the same is highlighted.

The rest of the paper is organized as follows. DC MGs IDSs and their advantages and disadvantages are presented in Sect. 2. Different types of passive IDSs for DC MGs are explained in Sect. 3, and active IDSs concepts and its types are reported in Sect. 4. At last, final conclusions are drawn in Sect. 5 with some future insights.

2 DC MGs Islanding Detection Schemes

Islanding detection methods which detect the islanding situation with fewer false positives is the leading research area. When the electrical system parameters crosses a certain threshold value, a trip signal is generated. Here, tripping time is the time which is required to successfully separate the two systems during islanding as reported in [18]. No fuse circuit breakers and solid-state circuit breakers are commonly used circuit breakers in DC MGs [19]. The author in [20] mentioned that in DC MGs, the detection time is with in 0.2 s. The advantages and disadvantages of DC and AC MGs IDSs are given in Table 1.

2.1 Intentional/Planned IDSs

Intentional/Planned IDSs are a detection method where generation and loads are scheduled prior to islanding. It means that which parts of the load to be isolated is decided before islanding [21, 22]. This type of detection technique is applicable to AC MGs as well as DC MGs. The leading cause of this type of islanding detection is a preplanned switching event. During such cases, the number of transients is less in MGs.

Table 1 Comparison between AC MG and DC MG IDSs

Parameters	AC MGs IDSs	DC MGs IDSs
Standards	Available (IEEE 1547)	Not available (Required Reconsideration)
System Parameters	Voltage, current, impedance, Active power, reactive power, frequency, harmonics, and phase	Voltage, current, active power, and impedance
IDSs available	Passive, active, and hybrid	Passive and active
Complexity	Easier than DC MG IDSs	Complex
Accuracy	Less accurate	Accurate
Tripping time	Less than 0.5 s	Less than 0.2 s

2.2 Unintentional/Unplanned IDSs

Unintentional/Unplanned IDSs are a detection method that is uncertain in nature. The leading cause of these type of IDSs is unplanned switching events [23, 24]. Islanding detection should be quick in order to maintain the reliability and stability of MGs, with a proper control strategy. In this case, the severity of the transients is more. During islanding conditions, electrical characteristics like current, voltage, impedance, frequency, active, reactive power output, etc., of DGs are changed significantly. In order to detect islanding, it is essential to observe the electrical parameters of the system continuously. IDSs are of two types, namely remote IDSs and local IDSs. The detailed classification is shown in Fig. 1.

Remote IDSs The communication medium between the grids and the DGs of MGs is required in this type of IDSs. Due to this, the cost of the islanding circuit increases, which is the major challenge of this type of IDSs. The examples of these IDSs, which are applicable for DC MGs are transfer trip, impedance insertion, and power line carrier communication (PLCC) IDSs. In transfer trip IDSs, supervisory control and data acquisition (SCADA) are used to monitor the status of circuit breakers and reclosures, which are present near to the point of common coupling (PCC) [25]. In the impedance insertion method, a low-value impedance is inserted nearer to the PCC in order to obtain proper power balance between generations and load [26]. In the PLCC method, a low energy signal transmits from the transmitter (utility side) to the receiver (DGs side). The disappearance of the signal represents the islanding condition [17]. Remote IDSs are more accurate and reliable than local detection schemes, but these are uneconomical because of their communication equipment.

Local IDSs Local IDSs utilize measurement and monitoring of electrical parameters like impedance, voltage, active power, etc., on the DGs side. The detailed classification of local IDSs is represented in Fig. 1.

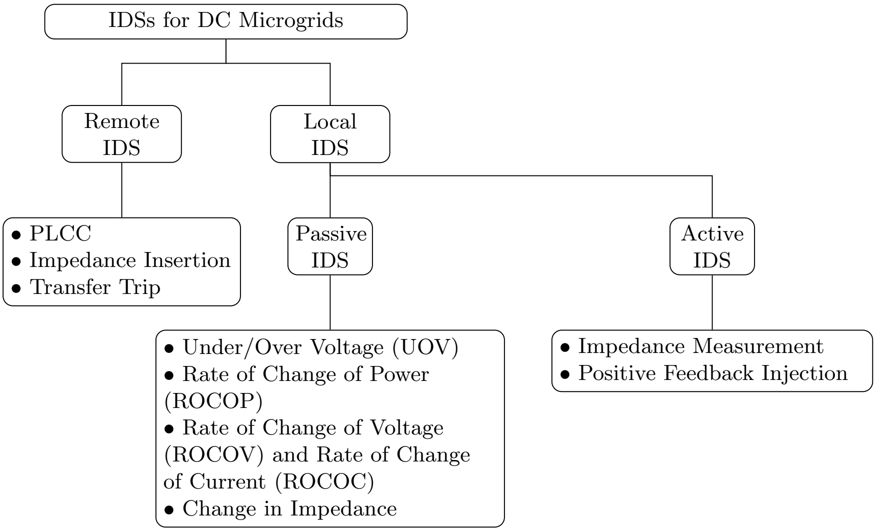

Fig. 1 Classification of DC MGs IDSs

3 Passive IDSs for DC MGs

Passive IDSs monitor the electrical system parameters like voltage, impedance, active and reactive power, frequency of DGs, etc., to identify the islanding. In DC MGs, the system parameters are voltage, impedance, and active power output of DGs. The islanding situation can be identified when the system parameters deviate from a predefined threshold value. In [27], passive IDSs for DC MGs have been explained. Note that, the implementation of passive detection schemes is simple and easy. Non-detection zone (NDZ) is the major challenge of this IDSs [28]. However, suitable threshold selection is also a complicated and challenging task.

3.1 Under/Over-Voltage-Based IDSs

In this type of IDS, it is required to sample the voltage v periodically and monitor to detect sudden changes in voltage in order to detect a fault condition. UOV IDS is important for grid-interfaced converters as the primary function of this type of converters is to maintain proper balance. A sudden change in voltage occurs commonly in the grid due to frequent removal and attachment of loads, so a threshold needs to be set to avoid faults [29]. The IDSs calculate the change in terminal voltage of DC/DC converter with t window length. Then, the obtained signal is compared continuously.