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Preface

This book explores the solutions on system and circuit level for hybrid resonant converters for portable applications operating from a Li-Ion battery (3.0–4.5 V) at power levels of a few hundred milliwatts. In particular, the growing field of wearables, for example, for medical monitoring devices and smartwatches, requires highly compact power supplies with high energy efficiency. The final goal for these space-constrained applications are fully integrated DCDC converters, which include all passive components either on-chip or by co-integration in the same package. Highly integrated state-of-the-art system-in-package solutions comprise inductive step-down converters, which operate in the lower MHz range with passive components in the order of μF and μH. In order to further scale down the size of passives, new conversion concepts are required. Hybrid switched-capacitor (SC) DCDC converters pursue a new and extremely promising approach by combining capacitor-based and inductive concepts in a single converter structure. Resonant operation of these hybrid converters allows for switching frequencies in the multi-Megahertz range (>10 MHz) at significantly reduced dynamic losses.

The objective of this book is to provide a systematic and comprehensive insight into design techniques for hybrid resonant switched-capacitor converters. Written in handbook style, the book covers the full range from fundamentals to implementation details including topics like power stage design, gate drive schemes, different control mechanism for resonant operation, and integrated passives. The material will be interesting for design engineers in industry as well as researchers who want to learn about and implement advanced power management solutions.

The main topics are as follows: (1) A new multi-ratio resonant converter architecture is introduced, which enables lower switching frequencies and better passive component utilization. This leads to high power efficiency as well as to full integration of all passive components. (2) The circuit block design for high efficiency of the power stage is investigated. (3) Implementation details and concepts for integrated passives are explored. (4) Different control mechanisms are derived, modeled, implemented, and compared to each other.

In particular, this book presents the first fully integrated resonant SC converter, which is extended by a multi-ratio power stage in order to cover the wide Li-Ion

input voltage range of 3.0–4.5 V. The design achieves a peak efficiency of 85% with an integrated 10 nH on-chip planar inductor (fully integrated) and 88.5% with a 10 nH in-package inductor (highly integrated).

Different control mechanisms are investigated and implemented by a fast mixed-signal controller. Switch conductance regulation (SwCR) operates at resonance frequencies as large as 47 MHz, which offers full integration of passives on IC level (no external components). In contrast, resonant bursting with dynamic off-time modulation (DOTM) achieves higher efficiency at the cost of an external output capacitor. The light load case down to currents as low as 0.5 mA is supported by automatic transition into pure non-resonant SC mode, controlled by frequency modulation.

Since there is no dynamic model available, yet, which allows to analyze the stability for this class of resonant SC converters, a model for the nonlinear mixed-signal control loop of the switch conductance regulation (SwCR) is proposed. The model enables stability analysis and allows for an optimal design of the control loop.

For the implementation of the power stage, the efficiency benefit of low-voltage transistor stacking over single high-voltage switches is investigated with a detailed but easy-to-use model of the transistor stack. A new implementation option for stacking of three low-voltage transistors for higher voltage capability is presented, which is independent of the input voltage. Finally, different concepts, implementation details, and achievable parameters of integrated passives (capacitors and inductors) for resonant SC converters are presented.

This book is based on our research at the Institute for Microelectronic Systems at Leibniz University Hannover, Hannover, Germany, in cooperation with Texas Instruments, Freising, Germany. We are grateful to many team members at the university as well as at our industry partner. Special thanks goes to Michael Lueders, Texas Instruments, for his constant interest in the topic and continuous support. He was always available for in-depth technical discussions, and his expertise in analog and power design was precious and helpful. We would like to convey many thanks to Dominique Poissonnier, Giovanni Frattini, and Erich Bayer for their invaluable advice and comments. We also want to thank Sebastian Beringer and Marc Christopher Wurz, Institute of Micro Production Technology at Leibniz University Hannover, for providing different microfabricated inductors for comparison and evaluation. We also appreciate the contributions of many students, especially the excellent work of Maik Kaufmann and Niklas Deneke.

A special thanks goes to our families, without their love and support this book would not have been possible.

Gomaringen, Germany — Peter Renz
Gehrden, Germany — Bernhard Wicht
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Contents

Acronyms

List of Abbreviations

BCD	Bipolar-CMOS-DMOS process technology
CMOS	Complementary metal-oxide-semiconductor
CPU	Central processing unit
DOTM	Dynamic off-time modulation
EEF	Efficiency enhancement factor
EMI	Electromagnetic interference
EME	Electromagnetic emission
ESR	Equivalent series resistance
FCML	Flying capacitor multilevel converter
FSL	Fast-switching limit
GMD	Geometric mean distance
GPU	Graphical processor unit
IoT	Internet of things
LDO	Low dropout regulator
MEMS	Micro-electrical-mechanical systems
MIM	Metal insulator metal
MOM	Metal-oxide-metal
MOS	Metal-oxide-semiconductor
NMOS	Negative-channel metal-oxide-semiconductor field-effect transistor
PCB	Printed circuit board
PMIC	Power management IC
PMOS	Positive-channel metal-oxide-semiconductor field-effect transistor
PMU	Power management unit
PWM	Pulse width modulation
QFN	Quad flat-no leads
ReSC	Resonant switched-capacitor converter
RMS	Root mean square
SC	Switched-capacitor converter

SiP	System-in-package
SMD	Surface-mounted device
SSL	Slow-switching limit
SoC	System-on-chip
SwCR	Swichted conductance regulation
ZCS	Zero current switching

List of Symbols

A_{Cfly}	m^2	Area consumption of flying capacitors
A_{eff}	m^2	Effective cross section area of bond wire
A_{L}	m^2	Area consumption of integrated inductor
α	F	Quality factor of integrated capacitor
C_{GS}	F	Gate-source capacitance
C_{GD}	F	Gate-drain capacitance
C_{DS}	F	Drain-source capacitance
C_i	F	Equivalent capacitance value in phase i
$C_{\square}$	$\mathrm{F/m}^2$	Capacitance density
C_{ox}	$\mathrm{F/m}^2$	Oxide capacitance per area
C_{p}	F	Pump capacitor
C_{eq}	F	Energy-based equivalent capacitance
C_{fly}	F	Flying capacitor
C_{fly1}	F	Flying capacitor 1
C_{fly2}	F	Flying capacitor 2
C_{fly3}	F	Flying capacitor 3
C_{BP}	F	Parasitic bottom plate capacitor
C_{SUB}	F	Parasitic substrate capacitance of inductor
C_{TP}	F	Parasitic top plate capacitor
C_{in}	F	Input capacitor
C_{out}	F	Output capacitor
C_{ox}	$\frac{\mathrm{F}}{\mathrm{m}}$	Oxide capacitance per area
δ	µm	Skin depth
$DLCR$		Dynamic load current range
E_i	J	Energy dissipation in phase i
ϵ_{o}	$\frac{\mathrm{F}}{\mathrm{m}}$	Permittivity of vacuum
$\epsilon_{\mathrm{r,oxide}}$	$\frac{\mathrm{F}}{\mathrm{m}}$	Relative permittivity of silicon dioxide
f_{clk}	Hz	Clock frequency of the oscillator
f_{sw}	Hz	Switching frequency
$f_{\mathrm{sw,res}}$	Hz	Resonance frequency
$f_{\mathrm{sw,res},1/2}$	Hz	Resonance frequency in ratio 1/2
$f_{\mathrm{sw,res},1/3}$	Hz	Resonance frequency in ratio 1/3
$f_{\mathrm{sw,res},2/3}$	Hz	Resonance frequency in ratio 2/3

$F_{\text{counter}}(s)$		Transfer function of the digital counter
F_{linears}		Combined transfer function of all linear components
$F_{\text{ReSC}}(s)$		Plant transfer function of ReSC converter
GM		Gain margin
GMD	m	Geometric mean distance
GND	V	Ground, global reference potential
G_{sw}	S	Switch conductance of the power switch
G_{LSB}	S	Least significant bit of the switch conductance
G_{offset}	S	Offset of the switch conductance
$G_{\text{sw,OP}}$	S	Conductance of the power switch at operating point
G_{LSB}	S	Smallest unity conductance value
I_i	A	Current in phase i
I_{in}	A	Input current of the converter
I_{RMS}	A	RMS current
I_{L}	A	Inductor current of the converter
$\hat{I}_{\text{L}}$	A	Inductor peak current of the converter
I_{out}	A	Output current of the converter
$I_{\text{out,max}}$	A	Maximum output current of the converter
$I_{\text{out,min}}$	A	Minimum output current of the converter
$I_{\text{out,OP}}$	A	Output current of the converter in the operating point
K_{Gsw}	S	Proportional term of the segmented power switches
K_{corr}		Correction factor for inductor
K_{Rout}	Ω	Proportional term for the equivalent output resistance
L	H	Inductor of resonant converter
L	m	Length of transistor
L_{s}	H	Self-inductance of a planar inductor
L_{model}	H	Inductance for dynamic model
l_{winding}	H	Total length of planar inductor
l_{w}	H	Side length of bond wire
M	H	Mutual inductance of wire segment
M_+	H	Positive mutual inductance
M_-	H	Negative mutual inductance
η		Efficiency
η_{CP}		Efficiency of charge pump
N		Conversion ratio
$N\left(\hat{x}_{\text{in}}\right)$		Describing function
P_{CBP}	V	Losses introduced by parasitic bottom plate capacitor
η_{LR}		Efficiency of linear regulator
η_{SC}		Efficiency of switched-capacitor converter
P_{cond}	W	Conduction losses of the power switches
P_i	W	Power dissipation in phase i
P_{loss}	W	Total power loss of the converter
P_{Rout}	W	Power loss due to equivalent output resistance
P_{sw}	W	Switching losses of the power switches
$P_{\text{sw,tot}}$	W	Total switching losses of the power switches

P_{tot}	W	Total losses of power switch
$P_{\text{LS,tot}}$	W	Total losses of the level shifters
P_{in}	W	Input power of the converter
P_{out}	W	Output power of the converter
PM		Phase margin
ρ	Ω m	Electrical resistivity
Q	V	Quality factor of inductor
r_{bond}	m	Radius bond wire
R_{BP}	Ω	Bond pad resistance
$R_{\text{DS,on}}$	Ω	On-resistance between drain and source
R_i	Ω	Equivalent resistance in phase i
R_{sw}	Ω	Switch resistance of the power switch
R_{offset}	Ω	Offset resistance of the power switch
$R_{\text{sw,OP}}$	Ω	Switch resistance of the power switch
R_{ESR}	Ω	Equivalent series resistance of inductor
R_{out}	Ω	Equivalent output resistance
$R_{\text{out,SC}}$	Ω	Equivalent output resistance in SC operation
$R_{\text{out,SSL}}$	Ω	Equivalent output resistance in slow-switching limit
$R_{\text{out,FSL}}$	Ω	Equivalent output resistance in fast-switching limit
$R_{\text{out,DOTM}}$	Ω	Equivalent output resistance in DOTM
$R_{\text{out,OP}}$	Ω	Equivalent output resistance in the operating point
T_{clk}	s	Period of the clock frequency of the oscillator
T_{I}	s	Integration time constant of the digital counter
t_{winding}	Ω	Thickness of the winding of the planar inductor
$t_{\text{winding,eff}}$	Ω	Effective thickness of winding
t_{ox}	m	Thickness of the oxide layer
V_{boot}	V	Bootstrapped voltage
VCR		Voltage conversion ratio
V_{blk}	V	Blocking voltage
V_{DD}	V	Positive supply voltage
V_{fb}	V	Feedback voltage for the control
V_{GS}	V	Gate-source voltage
V_{DS}	V	Drain-source voltage
V_i	V	Equivalent voltage across capacitor in phase i
V_{in}	V	Input voltage of the converter
V_{ref}	V	Reference voltage
$V_{\text{SS,HS}}$	V	High-side ground
$V_{\text{DD,HS}}$	V	Positive high-side supply voltage
$V_{\text{DD,LS}}$	V	Positive low-side supply voltage
V_{out}	V	Output voltage
V_{sw}	V	Voltage at the switching node
V_{th}	V	Threshold voltage of a transistor
W	m	Width of transistor
w_{winding}	m	Winding width of inductor
φ		Clock signal of the oscillator

φ_{CP}		Clock signal for the charge pump
φ_{SC}		Clock signal in SC mode
$\varphi 1_{\mathrm{SC}}$		Clock phase one in SC mode
$\varphi 2_{\mathrm{SC}}$		Clock phase two in SC mode
φ_{DOTM}		Clock signal in DOTM mode
$\varphi 1_{\mathrm{DOTM}}$		Clock phase one in DOTM mode
$\varphi 2_{\mathrm{DOTM}}$		Clock phase two in DOTM mode
$\varphi 1$		Clock phase one
$\varphi 2$		Clock phase two
φ_{CP}		Charge pump clock signal
μ_{n}	$\frac{\mathrm{cm}^2}{\mathrm{Vs}}$	Effective electron mobility
μ_{o}	$\frac{\mathrm{Vs}}{\mathrm{Am}}$	Magnetic permeability of free space
ζ		Damping factor of a resonant circuit

Chapter 1
Introduction

1.1 Motivation

Wearables and portable devices are an integral part of the Internet of things (IoT) with its vision that nearly every device and service is connected to the Internet as indicated in Fig. 1.1. All "*things*" connect, communicate, and coordinate with each other. This will transform the way we work and live. The worldwide market for wearables is expected to grow at an annual rate (CAGR) of 11.3% from 2019 to 2025 to reach $62.82 billion by 2025 [1].

While currently most of the wearables are used in simple wrist-mounted fitness trackers and smartwatches, future use cases may include smart glasses [2], smart headphones [3], smart shoes [4], smart clothes (e-textiles) [5], smart tattoos [6], or medical sensors and implants [7]. Wearables are expected to play a major role in areas such as communication, health monitoring, augmented reality, and authentication.

The rapid development of wearables and IoT devices toward miniaturized and power-efficient electronics can be considered to be similar to the evolution of the integrated circuit. Semiconductor technology scaling has enabled exponential growth of the transistor density, which has lead to significantly smaller and faster computing power over the last 60 years [8].

Higher integration brings several significant benefits. More functionality can be added together with even smaller form factors. This is especially important for portable applications where the available space is limited. Due to the shorter distance between functional blocks, the parasitics are reduced, which improves the system speed and performance.

Especially in mobile devices, multi-chip approaches have evolved to system-on-chip (SoC) or system-in-package (SiP) solutions that integrate the CPU, graphical processing unit GPU, memory, and analog and digital blocks all on one chip (SoC)

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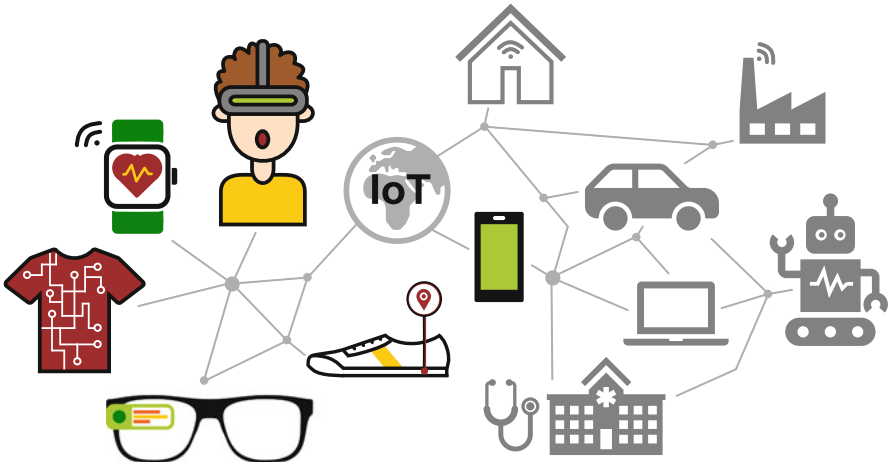

Fig. 1.1 Wearables and portable applications in the context of the IoT ecosystem

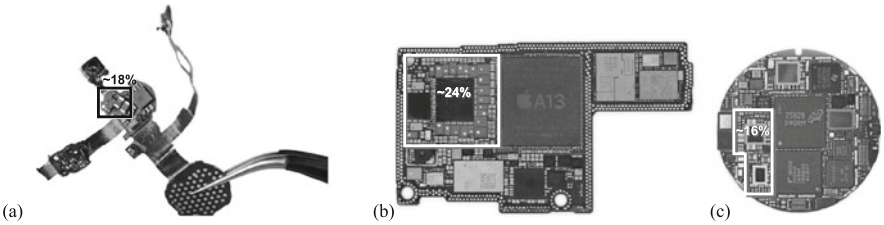

Fig. 1.2 Different main boards of wearable and portable devices. The occupied area by power management is marked with boxes. (**a**) Apple AirPods (smart headphone) [10]; (**b**) iPhone 11 Pro Max (smartphone) [11]; (**c**) Motorola Moto 360 (smartwatch) [12]

or in a single package (SiP). Thus, the main boards of the portable devices consist of fewer individual chips and passive components.

Power management units have resisted the integration and have shrunk in size only to a small extent [9]. They often consist of a power management IC (PMIC) with multiple integrated power stages, linear regulators (LDO), and control circuits. However, the passive components for energy storage, which are essential for the power conversion, are placed externally due to their large size. These passive components, mainly power inductors and capacitors, do not follow the scaling of Moore's Law [8] leading to a mismatch in future development.

Figure 1.2 shows different main boards of wearable and portable devices. While a lot of functionality (CPU, GPU, etc.) can be integrated in SoCs, the power management block (marked boxes in Fig. 1.2) still occupies a large PCB area, e.g., up to 24% in the iPhone 11 Pro Max. Especially the high number of external SMD inductors and capacitors around the PMIC is clearly visible in Fig. 1.2. Hence, the power management is still a major factor that determines the system size, which is a crucial parameter in wearable and portable applications.

Additional challenges arise for the power management systems since the number of voltage domains, the power demand, as well as the switching speeds will increase. This leads to a higher number of required DCDC converters. PMICs with external components require an increased pin count and degrade the performance due to interconnection parasitics and potential issues regarding electromagnetic interference (EMI).

The ultimate solution for these challenges is the full integration of the converters on a single chip. This can also reduce costs, increase reliability (due to lower component count and interconnections), and simplify the design for the user [13, 14]. The largest challenge for fully integrated conversion so far is the lack of high-quality inductors. Conventional converters all rely on at least one inductor. Only small inductance values are possible, which leads to very high switching frequencies, associated with high switching losses. This results in low efficiencies and limited voltage conversion ratios [15–21]. In recent years there is a growing interest in switched-capacitor (SC) converters due to their good integration capability in standard CMOS processes [22–32]. They can achieve high efficiencies at low output power, but they often do not support high-power operation. Moreover, SC converters do not have inherent regulation capability. Hybrid converters are a promising converter class that supports integration of inductive and capacitive components while minimizing losses and improving power density [33–41]. However, the requirements for the use in wearable and portable electronics are not met yet since low-power operation is often not supported and the input voltage range is limited (especially for fully integrated converters).

1.2 Scope and Outline of This Book

The scope of this work is summarized and depicted in Fig. 1.3. It is strongly related to the trend toward fully integrated power management with high efficiency, driven by portable and wearable IoT applications. DCDC converters are required for the down-conversion of a battery voltage to the supply voltages for both digital and analog circuits in processors and SoCs, which are continuously decreasing. This work covers fully integrated hybrid resonant DCDC converters in standard silicon technologies, which support a wide input voltage range of 3.0 to 4.5 V suitable for Li-Ion batteries and which also maintain high efficiency from high to low output power levels.

Requirements in terms of cost, small form factor, and better reliability are addressed by full integration of the power stage along with the required energy storage components such as capacitors and inductors. Very high switching frequencies (>100 MHz) are often used to scale down the size of the passive components, which in turn reduces the overall efficiency, especially at low output power levels.

In this work, the limitations of recent fully integrated DCDC converters are addressed by four main topics: (1) A new multi-ratio resonant converter architecture is introduced, which enables lower switching frequencies and better passive compo-

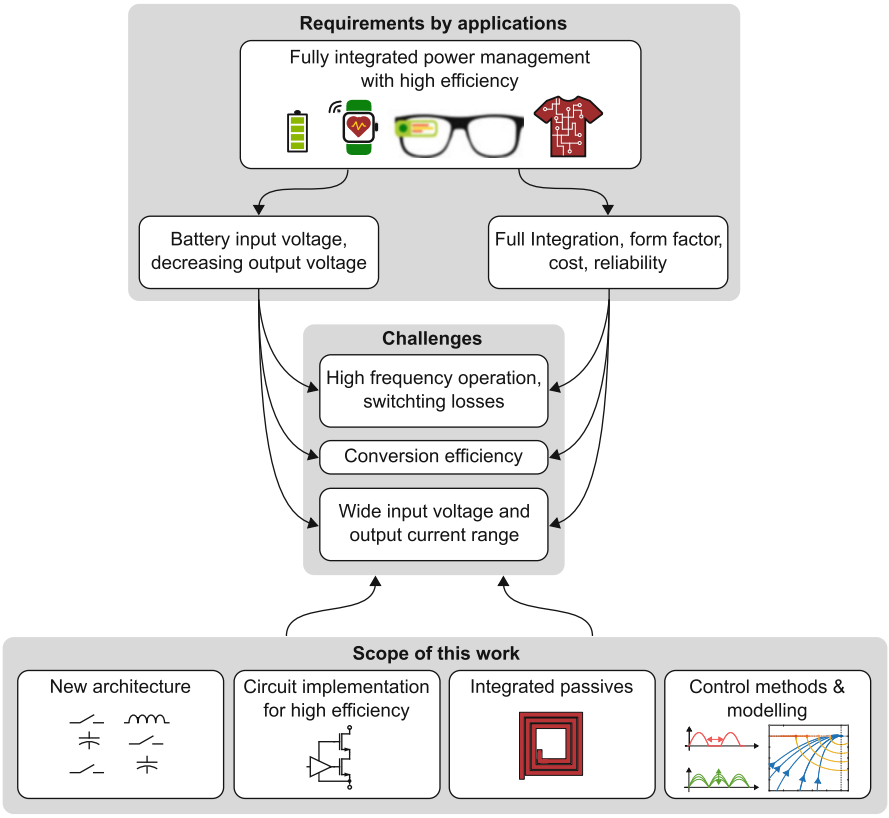

Fig. 1.3 Summary of the scope of this work

nent utilization. This leads to high power efficiency as well as to full integration of all passive components. (2) The circuit block design for high efficiency of the power stage is investigated. (3) Implementation details and concepts for integrated passives are investigated. (4) Different control mechanisms are implemented, modeled, and compared to each other.

The outline of this book is as follows. Chapter 2 highlights the motivation of this work and the demand for fully integrated power management for wearable and IoT applications. Section 2.2 gives an overview of different types of DCDC converters. Hybrid DCDC converters combine inductive and capacitive components while minimizing losses and improving power density. Different state-of-the-art DCDC converters with their pros and cons are compared. The hybrid resonant SC converter concept is the focus of this work since it shows the highest potential for fully integrated voltage conversion. The fundamentals of resonant SC converters are covered in Sect. 2.3.

The concept of hybrid multi-ratio resonant SC conversion is introduced in Chap. 3. Section 3.1 explains the basic topology for multi-ratio resonant conversion and the operation principle. Different control mechanisms depending on the size of the passive components are investigated in Sect. 3.2. An efficiency model for loss analysis and for finding of an optimal operation point is introduced in Sect. 3.3. Experimental results and a comparison to the state-of-the-art are presented in Sect. 3.4.

Chapter 4 explores the implementation and the control of the power switches, which is one of the key challenges for highly efficient converter operation. The efficiency benefit of low-voltage transistor stacking over single high-voltage switches is investigated in Sect. 4.1. Segmentation of the power switches, required for the proposed switch conductance regulation, is discussed in Sect. 4.2. Section 4.3 describes and evaluates different level shifter topologies. The generation of a flying gate drive supply is shown in Sect. 4.4, while Sect. 4.5 presents the full power stage implementation.

The implementation of the passive components plays an important role for fully integrated converters, covered in Chap. 5. Section 5.1 presents the design of loss optimized integrated flying capacitors. The modeling and implementation of integrated inductors are covered in Sect. 5.2. In addition, a comparison between fully integrated and off-chip inductors is shown.

Chapter 6 presents details on different control options for resonant SC converters. The implementation of two different control schemes is shown in Sect. 6.1 along with measured transient responses. A dynamic model of the resonant SC converter is introduced in Sect. 6.2, and the modeling of the nonlinear digital control loop for switch conductance regulation is discussed in Sect. 6.3. The model enables stability analysis and allows for an optimal design of the control loop. Experimental results verify the model.

Chapter 7 summarizes and concludes the results of this work.

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