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A Systematic and Multilevel Approach

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To Inês, Carlos, André, and Rita

F. Passos

To Judit and Nuria

E. Roca and F. V. Fernández

To Alejandro and Martina

R. Castro-López

Preface

Radio-frequency (RF) circuits are of utmost importance in applications developed for the Internet of Things (IoT), the fifth-generation (5G) broadband technology and electronic health (eHealth) monitoring. The design of RF circuits in nanometric technologies for IoT/5G/eHealth applications is becoming extraordinarily difficult due to the high complexity and demanding performances of such circuits/systems. Therefore, traditional design methodologies based on iterative, mostly manual, processes are unable to meet such requirements. Moreover, current EDA tools are getting outdated because they only support that kind of traditional methodologies. Also, the short time-to-market demanded by nowadays IoT/5G/eHealth applications is creating a design gap, thus leading to a productivity decrease in the deployment of such applications. Therefore, new design methodologies such as the ones proposed in this book are in need in order to increase the designer efficiency in the deployment of such applications.

This book focuses on ways to develop new design methodologies that allow the optimization-based synthesis of RF systems in a seamless, efficient, and accurate way. The supported basic idea is to develop methodologies based on the bottom-up hierarchical multilevel approach, where the system is designed in a bottom-up fashion, starting from the device level. Furthermore, at each level of the design hierarchy, several aspects must be taken into account in order to increase the robustness of the designs and increase the accuracy and efficiency of the simulations. The methodologies proposed in this book are able to handle circuit sizing and layout in a complete and automated integrated manner, in order to achieve fully optimal designs in much shorter times than traditional approaches. Moreover, the methodology also takes into account process variability. Therefore, it is possible to say that the overall goal of the book is to propose an efficient and accurate methodology able to automatically design RF systems, in which the upmost accuracy has to be guaranteed from the device to the system level. Throughout the book, strategies are proposed in each level of the hierarchy (from device to system level), augmenting the accuracy, efficiency, and the ability to achieve optimal results. Hence, the efforts were focused on the following directions:

- Development of accurate models for passive devices;
- Accurate and efficient synthesis methodologies for passive devices;
- Accurate, optimal, and efficient synthesis methodologies for circuits;
- Development of bottom-up design methodologies between the device and the circuit level;
- Development of variability-aware bottom-up design methodologies for RF circuits;
- Development of layout-aware bottom-up design methodologies for RF circuits;
- Development of layout-variability-aware bottom-up methodologies for RF circuits;
- Development of multilevel bottom-up design methodologies from the device up to the system level.

In order to show the innovative contributions in practice, the methodology developed is explained throughout the book, where each chapter focuses on different aspects of RF design. The book is organized as follows:

Chapter 1 explains the problematic issues in traditional design methodologies, discusses the automatic circuit design state-of-the-art and the demands for an accurate and efficient RF automatic circuit design methodology.

Since the methodologies developed in this book are applied to RF blocks present in RF receivers, Chap. 2 reviews the traditional receiver architectures and the three main blocks that constitute the RF front-end (low noise amplifier (LNA), voltage controlled oscillator (VCO), and mixer) are also described, as well as its most important performance parameters.

Chapter 3 discusses the development of accurate models for passive devices, where a novel surrogate modeling strategy for integrated inductors is presented for an accurate and efficient modeling. The presented model shows less than 1% error when compared to EM simulations while reducing the simulation time by three orders of magnitude. Several models were created for different inductor topologies and the accuracy and efficiency of such models enable its usage within iterative optimization loops for inductor synthesis. The same chapter presents accurate and efficient synthesis methodologies for passive devices. Furthermore, the surrogate model developed was used with multi-objective optimization algorithms in order to achieve Pareto-optimal fronts (POFs), which provide the best possible trade-offs for the inductor performances, e.g., inductance vs. quality factor vs. area. Obtaining such inductor POFs in an efficient and accurate manner is a key ingredient for the successful development of the multilevel hierarchical methodology presented in the book. Furthermore, SIDe-O, an EDA tool for the design and optimization of integrated inductors is presented. This tool offers an intuitive graphical user interface (GUI), which can be used by any RF designer in order to model, simulate, and design integrated inductors for different topologies, operating frequencies, and technological processes. Besides, SIDe-O also allows the creation of S-parameter files that accurately describe the behavior of inductors for a given frequency range, which can later be used in electrical simulations for circuit design in commercial environments. The surrogate models developed, and integrated in SIDe-O, provide

a solution to the problem of accurately and efficiently modeling inductors, as well as their optimization, alleviating the bottleneck that these devices represent in the RF circuit design process.

Chapter 4 regards the accurate, optimal, and efficient synthesis methodologies for RF circuits. In such chapter, a study is presented on how the inductor modeling error could impact the estimation of circuit performances. In order to do so, an inductor analytical model was compared against the previously developed surrogate model, and both were used in optimization-based circuit design approaches. It was proved that when used in the design/synthesis of RF circuits, analytical models, with typically high modeling errors, lead to suboptimal circuit designs, or, worse, to a disastrous non-fulfillment of specifications. Therefore, this states and reinforces the need for an accurate modeling of passive devices in RF, and therefore, the importance of the accurate inductor models illustrated in this book. Moreover, in all circuit optimizations, several simulation strategies were used in order to reduce the circuit simulation time and make optimizations more efficient. By using such strategies, some of the most expensive RF performances (e.g., third-order intercept point) can be efficiently calculated and considered during the automated design of RF circuits. In the same chapter, a wide study was carried out to compare two different optimization-based RF design methodologies: one based on hierarchical decomposition and bottom-up synthesis and another where synthesis was performed at the circuit level without hierarchical decomposition. In both cases, inductors were modeled using the same surrogate modeling strategy, and therefore, only efficiency and optimality were under comparison. It is demonstrated that bottom-up hierarchical design methodologies are far more efficient and are able to achieve superior results.

Chapter 5 presents a methodology where a layout-aware optimization is described which uses an automatic layout generation during the optimization for each sizing solution using a state-of-the-art module generator, template-based placer and router, which were specifically developed for RF circuits. The proposed approach exploits the capabilities of commercial layout parasitic extractors to determine the complete circuit layout parasitics. Also, in Chap. 5, the previously presented layout-aware methodology is further elaborated in order to take into account device process variability to develop a layout-corner-aware optimization.

Chapter 6 presents the multilevel bottom-up design methodologies which go from the device up to the system level. Such novel multilevel bottom-up circuit design methodology is described and applied to design an RF system composed of three blocks (an RF front-end composed of an LNA, a VCO, and mixer). This novel approach is disruptive because it covers the complete hierarchy of RF systems: starting at the device level, going up to the circuit level, and finally, reaching the system level. By using such multilevel bottom-up strategy, different circuits can be connected in order to build an RF system. Furthermore, each level of the hierarchy is simulated with the upmost accuracy possible: EM-level accuracy at device level and electrical simulations at higher levels. The methodology developed in this book encourages the hierarchical low-level POF reuse, which is typical in bottom-up

methodologies. Moreover, the methodology proved to be highly efficient for the design of RF front-ends for different communication standards, and, compared to alternative synthesis strategies, the presented methodology shows superior results.

In the end, Chap. 7 draws some conclusions.

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Contents

Chapter 1
Introduction

In an emerging telecommunications market, evolving towards 5G [1], it is estimated that there are over three billion smartphones users nowadays [2]. Only by itself, this number is astonishing. But nothing compares to what is going to happen in the foreseeable future. The next technological boom is directly related to the emerging internet-of-things (IoT) market. It is estimated that by 2020, there will be 20 billion physical devices connected and communicating with each other [3], which gives more than 2 physical devices per person on the planet. Due to this technological boom, new and interesting investment and research opportunities will emerge. In fact, it is estimated that in 2020 approximately three billion dollars will be invested in this market alone, 50% more than in 2017 [3]. Due to the fact that most of these IoT devices will have to communicate wirelessly among each other, and that radio-frequency (RF) circuits are essential for that purpose, there is, and there will be a high demand for RF circuits, nowadays and in the foreseeing years. Therefore, it is easy to understand why integrated circuit (IC) design companies specialized in RF, are already the companies which generate more income among all the fabless IC suppliers (e.g., Qualcomm and Broadcom, see Table 1.1).

The problem is that the design of RF circuits in nanometric technologies is becoming extremely difficult due to its increasing complexity. Designing an RF circuit is one of the most challenging tasks in nowadays electronics, partially due to its demanding specifications, convoluted trade-offs, and high operating frequencies. In fact, compared to its analog (baseband) and digital counterparts, the RF design requires a higher design effort despite the comparatively low number of devices (see Fig. 1.1). With todays' strict time-to-market restrictions and the need for design solutions with very demanding performance specifications, one of the areas where it is extremely important to focus is on the development of new systematic design methodologies for RF circuits. These RF circuit design methodologies must allow the designer to obtain circuits which comply with the demanding specifications in a reasonable time.

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Table 1.1 Illustration of the top 10 ranking of fabless IC suppliers for 2018 [4]

Rank	Company	Revenue
1	Broacom	18,941 M$
2	Qualcomm	16,370 M$
3	NVIDEA	11,163 M$
4	MediaTek	7882 M$
5	AMD	6475 M$
6	Xilinx	2868 M$
7	Marvell	2819 M$
8	Novatek	1813 M$
9	Realtek semiconductor	1518 M$
10	Dialog semiconductor	1443 M$

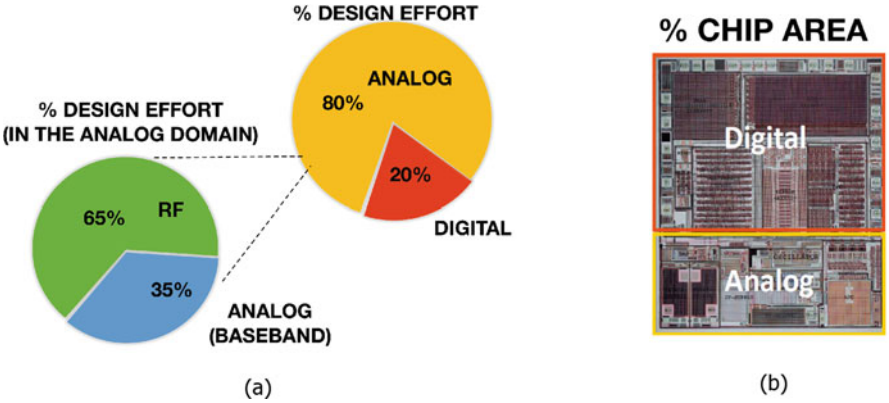

Fig. 1.1 (**a**) Illustration of the design effort comparison between analog and digital, and between analog (baseband) and RF. (**b**) Illustration of the area differences between the analog and digital parts

1.1 Traditional Design Methodologies

In the analog and RF domain, the traditional design methodology follows the flow illustrated in Fig. 1.2. The design of an IC starts by the definition of the circuit performances that have to be achieved, and then, the so-called electrical and physical synthesis have to be performed. These synthesis stages compose the core of any design flow and are the most important stages of any circuit design methodology. The first step of the flow is the electrical synthesis, where the designer must select an appropriate circuit topology and *size* the design. This *sizing* operation is a process where the designer finds the dimensions of each device used (transistors, capacitors, etc.) in order to meet the desired specifications. The output of this electrical synthesis is a schematic, which contains a list of all the devices composing the circuit and how they are connected. Furthermore, and more importantly, this schematic also includes the sizes of each single device (e.g., transistor lengths and

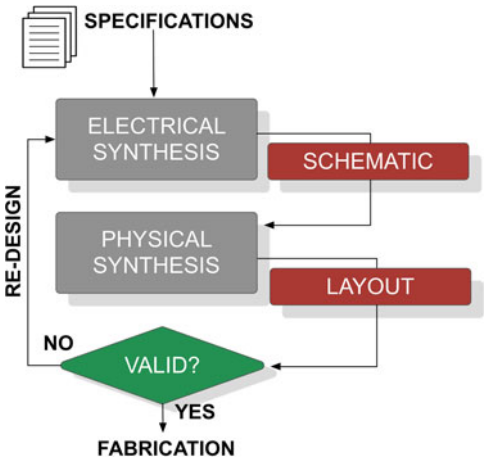

Fig. 1.2 Electrical and physical synthesis

widths, etc.). After the electrical synthesis is performed, the physical synthesis must be achieved. The goal of this step is to attain the physical representation of the circuit, known as *layout*. This layout is a collection of geometric shapes and layers which are later used for fabrication. After the physical synthesis, the layout of the circuit must be verified, and, if valid, it is ready for fabrication. If not, some re-design stages are needed.

If the circuit/system under design is too complex, analog/RF designers use divide-and-conquer techniques in order to reduce the complexity of the entire system. The basic idea is to partition the system into smaller pieces, which are easier to manage. This is known as hierarchical partitioning. The most well-known hierarchical design strategies are the top-down and bottom-up design methodologies, as shown in Fig. 1.3.

In top-down design methodologies, the designer starts by designing the system level, and the performances are consecutively derived for the lower levels, until reaching the device level. The circuit is designed in a more "abstract" way in high-levels, relying in e.g. behavioral simulations, and, at lower levels, more precise simulations can be performed. Furthermore, at each level of the design hierarchy, a verification must be performed in order to check if the design is valid. One of the advantages of top-down methodologies is that the performances for the entire system are known since an initial design stage (although only estimated). However, if any of the circuits composing the system do not attain the necessary performances, some re-design iterations are needed in order to achieve the desired specifications. In the worst possible scenario, the complete system architecture must be changed.

On the other hand, in bottom-up design methodologies, the design stage starts in the device level and ends up in the system level. The main disadvantage of bottom-up methodologies is that the system performances are only verified when all its composing blocks are designed, which can lead to major design changes later in the design process.

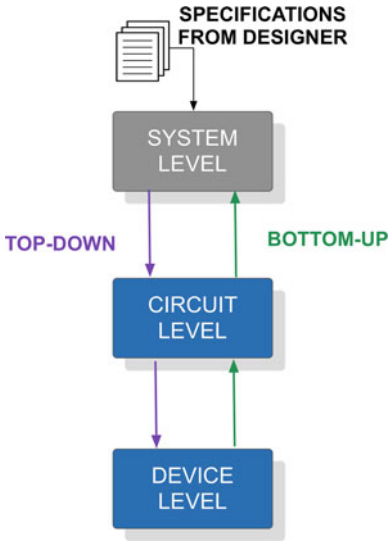

Fig. 1.3 Top-down vs. bottom-up design methodologies

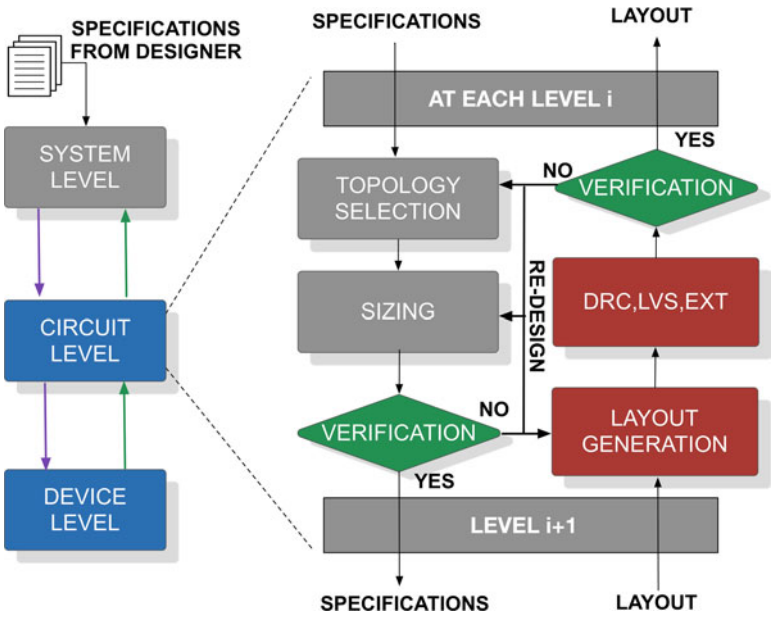

Fig. 1.4 General design flow for analog and RF integrated circuits

In practice, in traditional design methodologies, at each level of the hierarchy, the designer must perform a top-down electrical synthesis and a bottom-up physical synthesis, both needing a verification stage, as shown in Fig. 1.4.

As part of the electrical synthesis, the designer must select the architecture/topology which is capable of achieving the desired specifications. Afterwards, the sizing process is performed. At higher levels, the sizing is the process of mapping the current level specifications into the needed specifications for the immediately lower level. At device level, sizing is the process of dimensioning each passive and active circuit component. After the topology selection and sizing operation, the design is simulated and verified in order to check if the specifications are met. If the specifications are met, the flow continues to the next level.

The physical synthesis involves the layout generation stage, where the layout of a device, or circuit is generated. Afterwards, the layout is checked against a set of technology-defined rules with a design-rule check (DRC), and a layout-versus-schematic (LVS) check is performed, and if both checks are valid, the layout is acceptable for fabrication. Then, a parasitic extraction (EXT) must be performed. This is important in order to extract the layout-induced effects. These layout-induced effects add a set of *parasitic* capacitances, resistances, and inductances to the circuit, and therefore, may change its performances. If the specifications are not met after the layout extraction, the layout must be improved or, in a worse scenario, a re-sizing operation must be performed. The illustration of the complete hierarchical design for the levels of abstraction previously discussed (system, circuit, and device), is shown in Fig. 1.4.

All steps of the hierarchical flow shown in Fig. 1.4 can undertake several re-design iterations in order to reach the final system design that meets all specifications, therefore making the process of designing an IC a long and (usually) repetitive task. Hence, in order to relieve the designer from these long and repetitive tasks, the IC design process can be automated. In an ideal scenario, designers would have an electronic design automation (EDA) tool that could automatically perform the steps demonstrated in Fig. 1.4, something defined as a silicon compiler [5]. With this ideal tool, the user would only stipulate the desired specifications for his/her system and the tool would automatically generate the IC ready for fabrication. However, such a tool does not exist. In the digital domain the automatic circuit design tools are relatively close to the previously described silicon compiler. However, in the analog domain, and especially in RF, this silicon compiler is yet nothing but a dream.

Therefore, this book presents new systematic design methodologies capable of improving the state-of-the-art and cut short the distance between the RF and digital automatic design tools. By doing so, it will be possible to shorten the existing design productivity gap in RF circuit design.

In Sect. 1.2 a brief historical background on automatic circuit design is performed, and the current state-of-the-art is overviewed. In order to establish a new design methodology for RF systems, different bottlenecks of the RF design process must be addressed in order to successfully design such circuits. Hence, in Sect. 1.3, the demands for an accurate RF system design methodology are discussed.

1.2 Automatic Circuit Design State-of-the-Art

In this section, the state-of-the-art on automatic circuit design methodologies is reviewed. As previously mentioned, the electrical and physical synthesis are the core of any design methodology and, therefore, the state-of-the-art for both of them is reviewed.

1.2.1 Knowledge-Based Approaches

The basic idea of knowledge-based approaches is to have a pre-defined design plan, in the form of design equations or design strategies, to find the circuit sizing/layout so that the specifications are met. These type of tools are known as knowledge-based approaches because they use knowledge and expertise from the designer in order to establish/define a design plan for a given circuit.

1.2.1.1 Knowledge-Based Electrical Synthesis

In the 1990s, several tools were developed which could automatically perform electrical synthesis of analog circuits [6–10]. In these tools, the design plan was basically a set of analytical equations, which were used to solve the circuit. The tool provided the means to automatically execute a routine that would solve all the equations and, therefore, size the circuit under study. The main advantage of these approaches is its short execution time. However, deriving the design plan is hard and time-consuming, the derived equations are usually too simple and do not incorporate all the device physics. Moreover, the design plan requires constant maintenance in order to keep it up to date with technological evolution, and the results are not optimal, and only suitable for a first-cut design.

1.2.1.2 Knowledge-Based Physical Synthesis

In order to perform circuit physical synthesis, other knowledge-based tools were also developed. Roughly, the layout generation phases are *placement*, where all circuit components are distributed over the layout plane (also called floorplan), and routing, where all components are interconnected. Automatic knowledge-based layout generation tools were developed in order to generate the circuit layout in such a way that placement and routing were specified in advance. There are two types of knowledge-based approaches for automatic layout generation: rule-based and template-based approaches. Rule-based approaches use a set of rules that have to be followed by whichever placement and routing algorithms used during circuit layout generation [11]. In template-based approaches, the main idea is to capture the

designer expertise in a template that specifies all necessary component floorplanning and the routing spatial relationships. Moreover, the template must capture analog specific constraints like routing symmetry and device matching [12].

1.2.2 Optimization-Based Approaches

Knowledge-based design tools were developed in order to automatize some of the tasks inherent to analog/RF designers, without aiming at optimality. In order to reach optimal designs, optimization algorithms can be used in order to perform electrical/physical synthesis. The design of any circuit/system can be posed as an optimization problem, mathematically defined as,

$$\begin{aligned} \text{minimize} \quad & f(x); \quad \mathrm{f(x)} = \{f_1(x), f_2(x), \ldots, f_n(x)\} \in \mathbb{R}^n \\ \text{such that} \quad & g(x) \geq 0; \quad \mathrm{g(x)} = \{g_1(x), g_2(x), \ldots, g_m(x)\} \in \mathbb{R}^m \\ \text{where} \quad & x_{Li} \geq x_i \geq x_{Ui}, i \in [1, p] \end{aligned} \tag{1.1}$$

where x is a vector with p design parameters, each design parameter being restricted between a lower limit x_{Li} and an upper limit x_{Ui}. The functions f_j, with $1 \leq j \leq n$, are the objectives that will be optimized, where n is the total number of objectives. The functions g_k, with $1 \leq k \leq m$, are design constraints. The basic approach to solve Eq. (1.1) is illustrated in Fig. 1.5. It is possible to observe that the optimization algorithm is linked with a performance estimator, where the designer chooses the circuit performances to be considered (optimization objectives and constraints) and executes the algorithm which then returns the circuit sizing (e.g., widths and lengths of transistors).

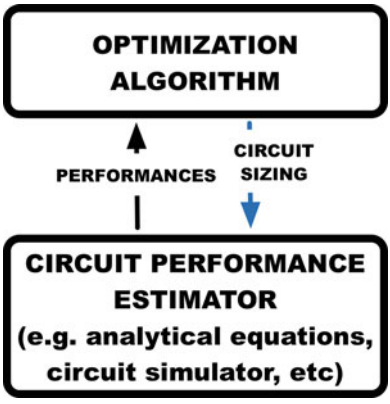

Fig. 1.5 Optimization-based methodology for circuit design

1.2.2.1 Optimization-Based Electrical Synthesis

While performing optimization-based electrical synthesis, there are two main categories, namely, equation-based and simulation-based.

The equation-based methods use analytical equations in order to evaluate the circuit performances. Several tools were developed which implemented this method [13–21]. Equation-based optimization-based sizing is similar to the knowledge-based sizing methods in the sense that they both use relatively simple analytical equations in order to estimate the circuit performances. However, equation-based methodologies do not need an explicit "design plan" to be defined. Also, the methods presented in this section go a step further by linking the equations with optimization algorithms, which were developed in order to reach optimal results. Similarly to the knowledge-based approaches, the advantage of equation-based methods is the short evaluation time. These methods are extremely suitable to find first-cut designs. However, like the knowledge-based approaches, the main drawback is that not all physical characteristics of the devices can be easily captured by analytic equations, making the method inaccurate (especially for RF circuits) and the generalization to different circuits, technologies, and specifications is very time-consuming because new equations must be derived.

Equation-based optimization methodologies are suitable because they are computationally cheap and, therefore, very fast to evaluate. However, they lack sufficient accuracy. Therefore, instead of using analytical equations in order to estimate the circuit performances, a circuit simulator (e.g., electrical simulator [22]) should be used in order to accurately estimate the circuit performances. The advantage is that these type of simulators tend to be much more accurate than analytical equations. The methods linking an optimization algorithm with a circuit simulator are usually defined as simulation-based strategies. Therefore, in order to obtain more accurate designs, this simulation-based optimization gained ground and became the most common optimization-based strategy. Some of the developed works that employ these simulation-based sizing methods can be found in [23–37].

1.2.2.2 Optimization-Based Physical Synthesis

Several tools have been developed that are able to perform physical synthesis using optimization-based approaches. With such tools, placement and routing stages of the layout generation are determined by an optimization algorithm according to a certain cost function. This cost function typically considers the minimization of some design aspect, such as, layout area or routing length. Furthermore, some constraints may be used in order to penalize the violation of some analog/RF design constraints, such as symmetrical RF signal paths, device mismatch, etc.

Some of the developed tools, the so-called heuristic approaches, are able to automatically generate layouts from circuit descriptions, while handling typical analog layout constraints such as, device matching, symmetry, etc. However, these approaches do not account for the performance degradation that appears due to