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Yield-Aware Analog IC Design and Optimization in Nanometer-scale Technologies

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Preface

Developments over the last decades in very large-scale integration technologies allowed meeting the increasing demand for faster, cheaper, and reliable electronic devices. One of the key factors to support those developments is the implementation of most high-level functions of the chip in digital circuitry, whose design is highly automated due to the adoption of mature electronic design automation (EDA) tools. While digital integrated circuits (ICs) design is mostly automated, its analog counterpart is supported by a set of independent tools, dedicated to each step of the design flow, and highly dependent on human intervention. The increasing demand in circuit performances and complexity of device models due to the aggressive IC technology down-scaling have led to the acceptance of new simulation-based optimization tools for analog IC sizing, thus increasing analog IC design flow efficiency. Most of those tools consider only nominal circuit parameters values during the optimization process. As devices shrink down into nanometer scale, the effects of process variation have become very important and not considering those effects during the optimization and sizing process may result in circuit solutions push to limits of performances and dangerously close to the boundary of feasibility. Therefore, including a prediction of the percentage of circuits that comply with circuit specifications after fabrication, i.e., the circuit parametric yield, in the sizing and optimization process is an important step to avoid expensive redesign iterations. Monte Carlo (MC) analysis is the most general and reliable technique for yield estimation, yet the considerable amount of time it requires has discouraged its adoption in population-based analog IC circuit sizing and optimization tools.

The new yield estimation methodology developed and presented in this book is able to reduce the time impact caused by MC simulations in the context of analog ICs yield estimation, enabling its adoption in optimization processes with population-based algorithms, such as genetic algorithm (GA), considering the yield as one of the optimization problem objectives. The proposed methodology reduces the total number of MC simulations required to evaluate the optimization algorithm population. The reduction in the total number of simulations is achieved

because at each GA generation the population is clustered and only the representative individual from each cluster is subject to MC simulations. Initial tests using a modified version of the k-means clustering algorithm, to identify similar individuals in the GA population, and a new technique to select the cluster representative individuals were able to achieve a reduction rate up to 91% in the total number of MC simulations, when compared to the number of MC simulations required to evaluate the complete GA population.

The need to balance the trade-off between yield estimation accuracy and the reduction rate of MC simulations made the k-means methodology to evolve and search for different clustering techniques. A new version of the developed yield estimation methodology with reduced time impact from MC simulations was finally developed and implemented in a state-of-the-art analog IC sizing tool using the fuzzy c-means clustering algorithm. The new methodology based on fuzzy c-means and named FUZYE is able to achieve good yield estimation accuracy and high reduction rates in MC simulations. The FUZYE methodology shows that the yield for the rest of the nonsimulated individuals in the population can be accurately estimated based on the membership degree of fuzzy c-means and the cluster representative individuals yield values alone. This new method was applied on several circuit sizing and optimization problems, and the obtained results were compared to the exhaustive approach, where all individuals of the population are subject to MC analysis. The FUZYE methodology presents on average a reduction of 89% in the total number of MC simulations, when compared to the exhaustive MC analysis over the full population. Moreover, other important clustering algorithms were also tested and compared with the proposed FUZYE, with the latest showing an improvement up to 13% in yield estimation accuracy.

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Abbreviations

AC	Alternate current
ACO	Ant colony optimization
ADC	Analog-to-digital converter
ADE	Analog design environment
ADS	Advanced design system
AIDA	Analog integrated circuit design automation
AMG	Analog module generator
AWE	Asymptotic waveform evaluation
BMF	Bayesian model fusion
BV	Basic variables
CAGR	Compound annual growth rate
CMOS	Complementary metal-oxide-semiconductor
CW	Cloud width
DAC	Digital-to-analog converter
DC	Direct current
DE	Differential evolution
DOE	Design-of-experiments
EA	Evolutionary algorithms
EDA	Electronic design automation
FCM	Fuzzy C-means
FoM	Figure-of-merit
FUZYE	Fuzzy c-means based yield estimation
GA	Genetic algorithm
GBW	Gain-bandwidth product
GDC	Gain DC
GP	Geometric programming
GSA	Gravitational search algorithm
GUI	Graphical user interface
HAC	Hierarchical agglomerative clustering

HAD	Hierarchical analog design
HSMC	High-sigma Monte Carlo
IBS	Importance boundary sampling
IBY	Individual-based yield
IC	Integrated circuit
ICs	Integrated circuits
IRDS	International roadmap for devices and systems
IS	Importance sampling
ISE	Infeasible solution elimination
KMD	K-Medoids
KMS	K-Means
LAA	Linear assignment algorithm
LDS	Low discrepancy sequence
LHS	Latin hypercube sampling
LNA	Low noise amplifier
LP	Linear programming
MADS	Mesh adaptive direct search
MC	Monte Carlo
MCS	Monte Carlo pseudo-random sampling
MOEA/D	Multi-objective evolutionary algorithm based on decomposition
MOPSO	Multi-objective particle swarm optimization
MOSA	Multi-objective simulated annealing
MPI	Message passing interface
NBV	Non-basic variable
NMOS	n-Channel MOSFET
NSGA-II	Nondominated sorting genetic algorithm-II
OAD	Orthogonal array design
OCBA	Optimal computing budget allocation
OO	Ordinal optimization
OpAmp	Operational amplifier
OPDK	Organic process design kit
ORDE	Optimization-based random-scale differential evolution
OTA	Operational transconductance amplifier
OTFT	Organic thin-film transistors
PAD	Procedural analog design
PC	Partition coefficient
PCA	Principal component analysis
PDF	Probability density function
PDK	Process design kit
PDKs	Process design kits
PE	Partition entropy
PLL	Phase locked loop
PMOS	p-Channel MOSFET
POF	Pareto optimal front

PRSA	Parallel recombinative simulated annealing
PSA	Pattern search algorithm
PSO	Particle swarm optimization
PVT	Process voltage and temperature
QMC	Quasi-Monte Carlo
RF	Radio frequency
RSM	Response surface methodology
s.t.	Subject to
SA	Simulated annealing
SBX	Single binary crossover
SoC	System-on-chip
SPS	Stochastic pattern search
SQP	Sequential quadratic programming
SR	Sparse regression
SSS	Scaled sigma sampling
SVM	Support vector machine
UD	Uniform design
VLSI	Very large-scale integration
WCD	Worst-case distance
WCP	Worst-case performance
WCPF	Worst-case pareto front
XML	Extensible markup language

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Chapter 1
Introduction

1.1 Variability Effects in Analog IC

The increased complexity in today's integrated circuits (ICs), where very large scale integration (VLSI) technologies progressed towards mixed-signal ICs, having digital and analog circuits coexisting on the same die as a complete system-on-a-chip (SoC) [1], allied to the adoption of smaller nanometer-scale integration technologies, creates new challenges to robust ICs design. Although the analog section occupies a small area in the entire chip, the analog design effort is considerably higher than the design of the digital blocks [2]. In traditional analog design, the designer achieves a valid circuit design configuration based on its knowledge and assisted by proper tools, like electrical simulators to validate the required specifications. This is usually a very time-consuming and error-prone iterative process, where a large number of specification constraints must be satisfied, like minimum DC gain, phase margin, and area. In today's competitive electronic market it is not enough to perform a basic circuit sizing process where only a feasible solution is found, i.e., a circuit sizing solution that fulfills all the required specification. Nowadays several of the specifications must be optimized, like power consumption and/or DC gain, which increases the complexity of manual design. Performing space exploration to achieve optimal circuit sized solutions has become a very hard task to IC designers. The increased number of variables and the highly nonlinear relation between circuit design variables and performance specifications brought by new smaller technology nodes made the use of an automatic circuit-level sizing and optimization tool, a requirement for satisfying the time-to-market pressure to release new and high-performance ICs.

Having automatic tools that can quickly provide a sized circuit solution or a set of solutions, when more than one objective is being optimized, is not enough. The economic pressure to produce affordable electronic devices revealed the need to fabricate more reliable circuit solutions. The inherently stochastic nature of semiconductor manufacturing processes led to the appearance of yield losses. The yield

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losses in silicon wafers that survive to production can be classified as *catastrophic* or *parametric* [3]. The catastrophic yield losses refer to functional failures, where the circuits do not work at all. These failures may be caused by short or open circuits. The parametric yield losses are caused by random and undesirable variations in circuit parameters due to nonideal fabrication processes, which lead to working and functional circuits that fail to comply with the required specifications. To improve productivity and avoid expensive redesign cycles it is important to predict the circuit parametric yield value during early stages of the circuit sizing processes. The parametric yield value refers to the percentage of circuits that are expected to comply with the required circuit specifications after fabrication. Technology scaling, the appearance of new materials and devices, combined with more demanding operating conditions, e.g., extreme temperatures and high radiation levels, poses new challenges to parametric yield estimation.

For several years, analog integrated circuit (IC) designers considered only global variations, or inter-die variations, and simulated the effects of these variations on the circuit performance by using corner analysis, which works well in digital project, but it is not enough to ensure that analog circuit performances are met after chip fabrication [4]. Analog ICs are also particularly sensitive to local variations, like devices mismatch effects, especially in the nanometer-scale integration technologies. Traditionally, the effects of local variations were prevented and corrected by the experience and know-how of the designer, which may lead to very conservative designs. In Table 1.1 it is possible to observe how the scaling effects impact the variability of the transistor threshold voltage standard deviation $\sigma(V_{\text{Th}})$ normalized by the threshold voltage for several nanometer technology nodes.

As a result of the increased impact of the variability effects, several techniques have been proposed to estimate the parametric yield. These techniques can be classified into two main categories: Monte Carlo (MC) based and performance model based.

MC analysis is considered the gold standard for parametric yield prediction, since it is the most reliable and accurate method to estimate the circuit parametric yield [6]. MC analysis performed in electrical simulators is based on statistical device models developed and tested by the technologies' foundries, which typically includes global and local variations. The main drawback of the MC approach is related to the high number of simulations needed in order to provide an accurate parametric yield estimation. The considerable amount of time needed to perform those simulations represents a huge obstacle to the adoption and integration of this type of approach in an electronic design automation (EDA) tool, since it would represent a severe bottleneck in the overall circuit synthesis process. In spite of all the drawbacks, the MC simulation-based yield estimation high accuracy keeps driving research in order to reduce its computational burden, which allows its adoption inside a yield-aware circuit sizing and optimization loop.

Table 1.1 Intra-die variability increase for the transistor threshold voltage parameter with CMOS technology node [5]

Technology node	250 nm	180 nm	130 nm	90 nm	65 nm	45 nm
$\sigma(V_{\mathrm{Th}}\ (\mathrm{mV}))/V_{\mathrm{Th}}\ (\mathrm{mV})$	$21/450 = 4.7\%$	$23/400 = 5.8\%$	$27/330 = 8.2\%$	$28/300 = 9.3\%$	$30/280 = 10.7\%$	$32/200 = 16\%$

1.2 Work Motivation

The International Roadmap for Devices and Systems 2017 (IRDS:2017) [7] identifies scaling as the first reason for the increasing reliability issues in new ICs technology integration nodes. Another identified cause for poor circuit reliability is premature aging, due to the long operation working cycles that electronics devices are subject in today's applications. To address this problem IRDS:2017 defends the need to investigate and develop new models, both statistical models of lifetime distributions and physical models of how lifetime depends on stress, geometries, and materials. The IRDS:2017 also points out the need for developing new reliability software tools with capabilities to predict and quantify the effects of variability during the design process. In addition to the IRDS:2017 concerns, Mladen Nizic, product marketing director at Cadence©, noted that "Advanced process nodes typically introduce more parametric variation, . . ., and other manufacturing effects affecting device performance, making it much harder for designers to predict circuit performance in silicon. To cope with these challenges, designers need automated flow to understand impact of manufacturing effects early, . . ." [8].

Analog ICs are expected to have the strongest relative growth of the IC market for the next five years. Power management, signal conversion, and automotive-specific analog devices will drive a compound annual growth rate (CAGR) of 6.6%, from $54.5 billion in 2017 to $74.8 billion in 2022, according to IC Insights [9]. In Fig. 1.1, the forecast CAGR of different product categories is compared with the expected CAGR of the total IC market growth of 5.1%. In order to keep driving this amazing growth, a considerable amount of time and work must be dedicated to improving the analog design flow and analog EDA tools.

The expected growth of the analog IC market and the challenging demand for new analog EDA tools, including early variability effects prediction in the design

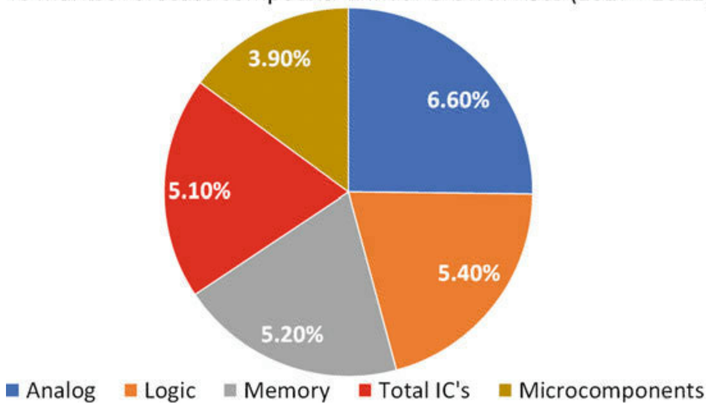

Fig. 1.1 Major IC categories market forecast compound annual growth rate for 2017–2022 (according to [9])

flow, are some of the major motivations for this work. Most of today's circuit sizing EDA optimization tools only performs some type of variability analysis at the end of the optimization process to validate solutions for yield requirements. This type of circuit sizing and optimization flow reduces the time impact of performing variability analysis at each optimization iteration but increases the probability of adding redesign iterations into the sizing processes. The development of a methodology using MC analysis for accurate yield estimation with reduced time impact in the sizing and optimization flow, although challenging, is a requirement to improve ICs reliability and cost efficiency in the manufacturing processes, especially at the new nanometer-scales technology integration nodes.

1.3 Work Purpose

The main goal of the work presented in this book is to develop an accurate yield estimation methodology in order to improve the robustness of circuit solutions sized in a state-of-the-art EDA tool. By improving solutions robustness, the analog IC production processes become more efficient, since expensive redesign iterations are avoided. The EDA tool considered for this work is a circuit sizing design automation solution known as AIDA-C [10–12]. The AIDA-C circuit sizing tool is a simulation-based, multi-constraint, and multi-objective optimization tool, whose optimization kernel is based on evolutionary techniques. Since MC-based approaches are considered the most accurate methods for yield estimation, this work develops its new methodology based on MC analysis. To further improve the yield estimation accuracy, MC analysis will be based on electrical simulations using the trustworthy industry process design kits (PDKs) statistical models.

Combining MC analysis for yield estimation with a population-based evolutionary optimization algorithm, where each population individual is evaluated through electrical simulation, may represent a huge bottleneck in the overall optimization process. Reducing the time impact caused by MC simulations is possible by performing less simulations or iterations, as many electrical simulators call them, to each individual in the population. Another approach is selecting some relevant individuals from the population and performing MC analysis only to those individuals. Since the approach of performing less simulations would reduce the yield estimation accuracy, this type of approach was discarded.

According to the requirements presented so far, the new yield estimation methodology must satisfy the following conditions:

1. Adopt MC analysis to estimate the yield.
2. Perform MC simulations in a commercial electrical simulator with standard PDKs statistical models, for more accurate results.
3. Completely integrate a yield estimation methodology in the optimization loop of a population-based optimization analog IC sizing tool.