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Thierry Di Gilio
Andreia Cathelin *Editors*

# The Fourth Terminal

## Benefits of Body-Biasing Techniques for FDSOI Circuits and Systems

Springer

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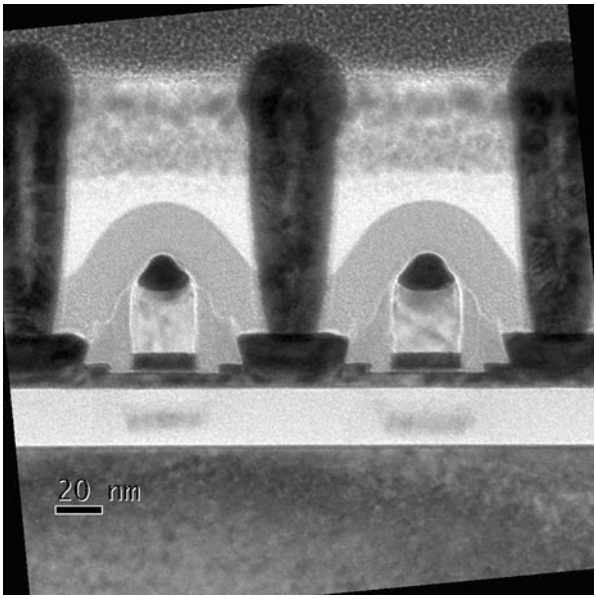
*To our families.*




FD-SOI transistor TEM, the transistors' channel is the volume between the gates and the white colored buried oxide. Copyright STMicroelectronics. Used with permission

# Foreword

This book deals with applying a voltage potential to the volume below the buried oxide in the TEM adjacent photography, and this modulates transistor's $V_T$; hence, the motto "FD-SOI Body-Bias enables software defined $V_T$."

Crolles, France — Sylvain Clerc
Crolles, France — Thierry Di Gilio
Crolles, France — Andreia Cathelin
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# Contents

# Acronyms

| | |
|---|---|
| ABB | Adaptive body-biasing |
| AC | Alternative current |
| ADC | Analog to Digital Converter |
| ALU | Arithmetical and logical unit |
| ATPG | Automatic Test Pattern Generator |
| AVS | Adaptive voltage scaling, can be static of dynamic |
| BBCO | Body-biased-controlled oscillator |
| BBG or BBGEN | Body-bias generator |
| BEOL | Back-end-of-line |
| BIST | Built-in Self Test |
| BJT | Bipolar junction transistor |
| BL | Bit line |
| BLE | Bluetooth Low Energy |
| BLM | Bit line margin |
| BOX | Buried oxide |
| BPPM | Burst-pulse position modulation |
| BPSK | Binary Phase-Shift Keying modulation |
| BTI | Bias Temperature Instability |
| BW | Bandwidth |
| CAD | Computer-Aided Design |
| CG | Common gate |
| CPR | Critical path replica |
| CPU | Central processing unit |
| CPW-G | Grounded coplanar line |
| CS | Common source |
| CSR | Control and status register |
| CTAT | Complementary to absolute temperature |
| DAC | Digital to Analog Converter |
| DC | Direct current |
| DC-DC | DC to DC (converter) |
| DCO | Digitally controlled oscillator |

| | |
|---|---|
| DFT | Design for Test |
| DIBL | Drain-induced barrier lowering |
| DLL | Delay locked loop |
| DRM | Design Rules Manual |
| DUT | Device under test |
| DVFS | Dynamic voltage and frequency scaling, this is nonstatic AVS |
| ECO | Engineering change order |
| EDA | Electronic Design Automation |
| EM | Electromagnetic |
| ESD | Electrostatic discharge |
| EWS | Electrical Wafer Sort test |
| FA | Full-adder |
| FBB | Forward body-bias |
| FD-MIMO | Full Duplex Multiple Input Multiple Output |
| FF | Flip-Flop or Fast-Fast process |
| FIFO | First in first out |
| FOM | Figure of merit |
| FOx | Fan-Out-of-x ($x$ can be 2, 3, 4, ...) |
| FS | Fast N, Slow P process corner |
| FSM | Finite state machine |
| GSG | Ground signal ground |
| HA | Half-adder |
| HCI | Hot carrier injection |
| HF | High frequency |
| HVM | High volume manufacturing |
| HVT | High VT |
| IIP2 | Second-order Input Intercept Point |
| IO | Input/output |
| IP | Intellectual property (circuit) |
| IR | Impulse Radio |
| ITRS | International Technology Roadmap Standard for Semiconductors |
| L | Transistor Length |
| LDO | Low DropOut (regulator) |
| LFN | Low frequency noise |
| LFSR | Linear feedback shift register |
| LO | Local oscillator |
| LPDDR | Low Power Dual Data Rate (Memory) |
| LSB | Least significant bit |
| LUT | Look-up table |
| LVT | Low VT |
| MC | Monte Carlo |
| MHC | Model to Hardware Correlation |
| MIM | Metal-insulator-metal (capacitor) |
| MOM | Metal-oxide-metal (capacitor) |

| | |
|---|---|
| MS | Microstrip (line) |
| MSB | Most significant bit |
| NBTI | Negative Bias Temperature Instability |
| OTA | Operational transconductance amplifier |
| P.V.T.a. or PVTA | Process voltage temperature and temperature (variations) |
| PA | Power amplifier |
| PAE | Power-added efficiency |
| PB | Poly Bias, MOS length optical deshrink, PB4 means effective length is drawn L + 4 nm |
| P-Cell | Parameterized cell |
| PG | Pulse generator |
| PHY | Physical layer |
| PLL | Phase locked loop |
| PCB | Printed Circuit Board |
| PMU | Power management unit |
| PRF | Pulse repetition frequency |
| Psat | Saturated (output) power |
| PSD | Power spectral density |
| PSRR | Power supply rejection ratio |
| PTAT | Proportional to absolute temperature |
| PVT | Process Voltage Temperature operating point |
| QoR | Quality of Result |
| RA | Read ability |
| RBB | Reverse Body-Bias |
| RF | Radio-frequency mmW millimeter-wave |
| RO | Ring oscillator |
| RS | Read stability |
| RVT | Regular VT |
| SC | Switched-capacitor |
| SF | Slow N, Fast P process corner |
| SiGe | Silicon Germanium |
| SNM | Static Noise Margin |
| SOA | Safe-operating area |
| SoC | System on a Chip |
| SOF | Sign-off |
| SS, SF, FS, FF | Slow-slow, slow-fast, fast-slow, fast-fast (process corners) |
| SS | Slow N, Slow P process corner |
| STA | Static Timing Analysis |
| TA | Application temperature |
| TCR | Temperature coefficient of resistivity |
| TD | Thermal diffusion |
| TDC | Time-to-digital converter |
| TDDB | Time Dependent Dioxide Breakdown |
| THz | Terahertz (frequency) |
| Tj | Junction temperature |

| | |
|---|---|
| TL | Transmission line |
| TRC | Tunable replica circuit |
| TTF | Time To Failure |
| TX | Transmitter |
| ULP | Ultra low power |
| USL | Upper specification level |
| UTBB | Ultra-thin body and box (FD-SOI) |
| UWB | UltraWide band |
| $V_{Tinv}$ | Voltage of temperature inversion same as ZTC |
| Vbb | Body-Bias voltage |
| VCDL | Voltage-controlled delay line |
| VMU | Vector memory unit |
| VRU | Vector roundhead unit |
| VSWR | Voltage standing wave ratio |
| VT | Threshold voltage |
| VXU | Vector execution unit |
| W | Transistor width |
| WM | Write margin |
| WS | Write stability |
| ZTC | Zero-temperature coefficient |

# Chapter 1
# Introduction


**Andreia Cathelin and Sylvain Clerc**

## 1.1 Foreword

The CMOS integration race has reached limitations for planar silicon process starting from the 40 nm node. The transistor channel was more and more difficult to control and specific process integration methods such as pocket implant, silicon strain, and lightly doped drain were introduced to enable devices' good carrier mobility and electrostatic control, are moreover this type of process integration could not be successfully continued after the 20 nm node. Starting from the 28 nm node a consensus solution emerged consisting in the use of fully depleted active devices either fully depleted silicon on insulator (FD-SOI) or Fin-FET. While the fundamental physics laws are similar for these two big families of devices, the process integration is much different and had to bring the process engineers from the well-known planar technologies (applies also for FD-SOI) to fully 3D structures (for Fin-FET).

As we will largely discuss all over the different chapters of this book, all FD-SOI technologies are *planar* and offer to designers a brand new operation playground by the fact that the transistors in this technology have now *4 effective terminals*: source, drain, gate, and body – the volume underneath the conduction channel. In FD-SOI, by applying a voltage bias on this latest, one can efficiently vary the transistor's threshold voltage. While this technique is not new [1] it is the first time it can be deployed with a large electrical impact into commercial CMOS technology.

All design techniques existing in classical planar CMOS technologies since more than 30 years can now be revisited and brought to a higher level, by adding a new and efficient tuning knob, the transistor's body tie, inside all the schematics.

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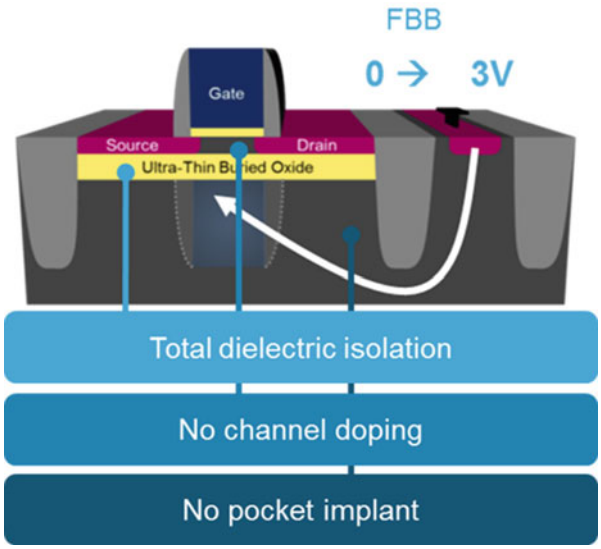


**Fig. 1.1** A generic cross-section of an UTBB FD-SOI transistor. ©2017 IEEE. Reprinted with permission

The circuit designer can now control on the fly the transistor's threshold voltage variation by software commands. It brings in to all types of schematics, from analog to RF, mmW to mixed signal, digital and memories, a new degree of design freedom. Its integration into low power CMOS technologies offers fantastic integration framework for all kinds of IoT, 5G and any other type of energy efficient circuits and systems.

The aim of this book is to introduce to the design community the straightforward design solutions in any modern FD-SOI planar CMOS technologies, by taking full advantage of body-biasing techniques to efficiently modulate on the fly SoC solutions from high performance operation to energy efficiency mode. All design techniques are based on the classical pillar of regular planar CMOS devices. As the first fully industrial solution has been the 28 nm FD-SOI CMOS technology from STMicroelectronics, all the design examples given in this book have been demonstrated within this process integration frame.

Figure 1.1 gives a generic cross-section of a FD-SOI CMOS device [2]. This technology is called ultra-thin body and BOX (UTBB) FD-SOI CMOS, as in the 28 nm node the active device has an ultra-thin conduction film (7 nm) and lays atop a 25 nm insulation layer of buried oxide (BOX). This planar topology's direct implications are the following: thanks to the SOI BOX layer, the transistor gets total dielectric isolation. No channel doping is needed as thanks to the thin silicon film, the channel is fully depleted. Also enabled by this topology, no pocket implants are needed for the source and drain, which enhances naturally the analog/RF transistor's behavior. Another implication of the thin BOX layer is the fact that the front-side

transistor's electrostatics can be controlled from underneath the BOX (area called transistor body). By applying a voltage on the transistor body, one can change or modulate the threshold voltage of the main (front-side) transistor. We can see this device as well as a planar dual-gate device: the front-gate is the regular one (like in bulk technology) and the second one comes from the body tie, with the BOX as the back-side gate oxide. As the thickness ratio of the front and back gate oxides is about 10, the front-side transistor's transconductance *gm* is 10 times bigger than the one of the back-side gate.

Body-bias can be applied in two directions: either to lower devices threshold voltage, with PMOS body terminal driven to a lower voltage than source supply (VDD) and NMOS body driven to a higher voltage than source supply voltage (usually ground), this is forward body-bias. This leads to a *high performance* type of operation. Reversely, body-bias can be applied to increase devices threshold voltage, with PMOS body terminals drive to a higher voltage than VDD and NMOS body terminal drive to a lower voltage than supply (i.e., negative voltage), this is reverse body-bias. This enables a *low leakage* energy efficiency type of operation.

When applied to bulk technology, the forward body-bias voltage range is limited by junction diodes on-current and latch-up sensitivity, reverse body-bias is accessible to bulk technology without latch-up risk but is limited by gate induced drain leakage (GIDL). As will be exposed in Chap. 2 detailing the device microstructure, the FD-SOI technology enables a wide range of body-bias voltages because its intrinsic channel isolation overcomes the bulk technology bias range limitations of both GIDL and latch-up.

## 1.2 Analog Design Aspects

In the analog/RF design application domain, the historical nanometer downscaling roadmaps have accustomed analog designers to have transistors' analog behavior degraded from node-to-node because of digital low-power and high-speed objectives needing the above-mentioned process integration techniques. While this can be overcome in deep-submicron CMOS by introducing analog specific devices (like having no pocket implants), in FD-SOI technology the thin film structure inherently eliminates many of the analog performance limitations and permits to have better DC gain behavior and higher current drive capability [3]. As well, the transistors implementation with thin film layers permits to limit the important variability effects present in such nm nodes. The presence of the SOI topology naturally limits the parasitic effects, hence we get higher achievable bandwidth or a lower power consumption for a given operation bandwidth. As it will be largely developed over the next chapters, in FD-SOI voltage biasing range on the transistor's body is very wide (almost |3 V|), whereas in a regular CMOS process it is only of few tenth of mV. This, in conjunction with a higher body effect, enables an unprecedented tuning range of the threshold voltage of more than 250 mV.

In terms of high frequency capability, the 28 nm CMOS node permits to obtain transition frequencies of around 300 GHz, which hence enable operation from RF domain up to mmW frequencies, such as the recently investigated communication bands at 60 GHz and above, for 5G high data rate applications.

Regarding ultra-low power solutions tailored for IoT applications, FD-SOI technologies are as well the sweet spot for ultra-low voltage flexible and energy efficiency implementations.

Furthermore, body-biasing enables either statically or dynamically, via embedded voltage generators, to compensate for environmental conditions and/or reconfigure/tune analog design features depending on application and usage. As well, this huge optimization domain offered by the wide body-biasing range permits to propose new design schemes with much reduced design margins, hence with smaller power consumption and reduced chip area. Simple CMOS inverter based transconductor schematics can be efficiently revisited for class A or AB amplifiers, and the classical differential pair can now be given new dimensional design heights by simply tuning its body ties. New kinds of closed-loop tuning and trimming schemes can be proposed to ensure an efficient in specifications operation of full analog/RF/mixed signal SoCs.

## 1.3 Digital Design Aspects

Looking back at the past 20 years, the digital designers have faced the following trends:

- increased interconnect delay versus gate delay which lowers custom digital added value
- increased local mismatch affecting SRAM write margin, non-CMOS Flip-Flops robustness, and constraints closure of synchronous digital parts
- transition from 1D device to 2D device with increased influence of lateral electric field on channel control, causing $V_T$ roll-off and drain-induced leakage (DIBL)
- increased power density as device dimensions shrink faster than power

These factors have some interdependence, for example, the increased local mismatch weakness has prevented the digital bitcell to shrink at the same rate as the gate length [4], and increased the leakage because of lower $V_T$ needed. To address increased leakage and dynamic power density, various design approaches have been put in place: multi $V_T$ design, retention and power gating, multi-VDD, and adaptive voltage scaling (AVS). Among these techniques, early body-bias usage can be traced back in memory design [5]. It has emerged in the years 1990–2000 in digital when some hardware operator and microprocessor designs were reported using this technique [6–8]. However, the body-bias tuning range has lowered with technology shrink in bulk technologies. The relative merit of AVS compared to bias was studied in [9] but with limitation of bias dynamic and PMOS tuning only. It will be exposed how FD-SOI technology recovers back body-bias tuning range.

## 1.4 Book Overview

This book is structured in three parts as follows:

The first part presents a technology overview (Chap. 2), general considerations on what body-biasing can bring to the digital and analog designers (Chaps. 3 and 4) and SRAM bitcell design under body-biasing conditions (Chap. 5).

The second part presents a selection of circuits which illustrate the body-biasing usage in various fields, from analog to RF/mmW and digital, and from building blocks to circuits and SoC implementations. The choice of topics is non-exhaustive, they present some design fields where fully aware body-bias design can change significantly the game and permit to get straightforward competitive advantages. All presented design solutions, validated through silicon implementation, show best-in-class performance, and outperform state of the art by taking full benefit of body-biasing deployment.

Chapter 6 presents an analog/high-speed circuit block for wide range and fine grain programmable delay elements, very useful for high data rate communications both wired and wireless.

Chapters 7 and 8 bring highlight in mmW design solutions, with implementations showing some very high frequency mmW oscillators implementations (up to 200 GHz) and 30 GHz 5G mmW power amplifiers. Both active devices behavior at high signal level at mmW frequencies and passive elements integration with sufficient quality factor, in a dense back-end-of-line (BEOL) VLSI technology, are tackled in these two chapters.

Chapter 9 gives a detailed insight on an RF wireless sensor node IoT transmitter SoC with analog/RF/mixed signal and digital circuitry.

Monitoring is key for body-bias deployment as will be exposed in the following Part III, to this end, an energy efficient thermal sensing is presented in Chap. 10.

Full SoC implementations of several generations of RISC-V processors are then detailed in Chap. 11, demonstrating energy efficiency giga operations per seconds scale computing (GOPS).

The third section of this book presents the body-biasing deployment in mixed-signal and digital SoCs.

This part includes body-bias control designs based on either closed-loop (mid- to long-term solutions, Chap. 12) and open-loop (seen as short-term industrial perspective, Chap. 13).

Energy efficient design has been a design priority for decades now and it will see its full deployment through all the panel of applications covered by IoT implementations, in this sense modulating the devices Ion is a must have. Body-bias is an alternative to the well-known adaptive voltage scaling (AVS) technique, both have their pros and cons and can be eventually mixed, this subject will be covered in Chap. 14 together with a review on open-loop and closed-loop body-bias control solutions.

We study also body-bias voltage generation units for digital usage (Chap. 15), and review on the practical side, digital design flow methodology (DDFM) specific aspects (Chap. 16).

Through this set of design examples from small circuits up to SoCs, we are illustrating the power-performance-area (PPA) benefits which can be gained by body-biasing techniques in FD-SOI technologies and help the reader make the appropriate architectural choices for their own designs. We wish you an enjoyable journey through the art of body-biasing!

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# Part I
# Device Level and General Studies for Analog and Digital

# Chapter 2
# FD-SOI Technology


**Franck Arnaud**

## 2.1 Introduction

Whatever the type of applications, from internet-of-things to automotive microcontrollers, we anticipate a strong demand in terms of power reduction, frequency increasing, and analog mixed signal co-integration. Consequently, advanced CMOS technologies have to adapt the offering with respect to customer demand with a limited rework in terms of design (library and complex IPs). A simple way, already well known and used, is the adaptive voltage scaling (AVS) technique, based on power supply ($V_{dd}$) modulation, depending on the type of application or need. Thus, with a same set of foundation IPs and an identical technology, we can extend the range of applications served. Even if AVS is very powerful, especially in terms of digital speed, we do see three major drawbacks: active power rising, severe transistor and wiring reliability degradation, and no intrinsic improvement for analog blocs.

Moving along from bulk-planar transistor toward FD-SOI-planar one and the FBB technique, we have the opportunity to provide the same level of design flexibility as AVS but without the drawbacks depicted previously. The main technical advantage of FD-SOI is the threshold voltage modulation of the device. It means we have a knob, thanks to gate bias, to change the intrinsic positioning of the device. Threshold voltage ($V_T$) reduction improves the speed of the device, especially at low voltage operation, feeding digital performance request. If no extra frequency is required, then we have the opportunity to drop the power supply itself to mitigate the power consumption. And for analog circuits, $V_T$ lowering will bring higher *gm* without transistor mismatch degradation. Finally, threshold voltage reduction does

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not hurt device reliability due to the fact that both lateral and vertical electrical fields are maintained.

In this chapter, we will first describe the physical structure of the device and provide the basic equations of the $V_T$ modulation of FD-SOI transistor. The role of the back gate will be properly described and explained. Device structure comparison will be presented versus reference bulk-planar architecture. Section 2.3 will be dedicated to the native impact of the FBB on a single transistor. Basic transistor parameters will be reviewed such as $V_T$, drive current ($I_{\text{on}}$), or quiescent one ($I_{\text{off}}$) completed with a first dynamic analysis based on ring oscillator (RO) design. Transistor variability tightening will be discussed in Sect. 2.4 evidencing the superior of FBB to compensate intrinsic process variability. Sections 2.5 and 2.6 will focus on digital and analog figures of merit, respectively. Digital part will be dedicated to the power reduction thanks to FBB solution. FD-SOI architecture and body-biasing capability for 6T-SRAM bit-cell will be reviewed and deeply discussed in Sect. 2.7. Finally, reliability results will be presented in the last section of this chapter focusing on the technology.

**Notation**

Throughout this chapter, the classical notation applies [1, 2]:

| | |
|---|---|
| $\phi_m$ | metal work-function |
| $\phi_{fb}$ | Flat band voltage |
| $\psi_s$ | Silicon gate-side surface potential |
| $\psi_{sb}$ | Silicon body-side surface potential |
| $E_C$ | Silicon bottom conduction band energy level |
| $E_V$ | Silicon top valence band energy level |
| $E_i$ | Intrinsic energy level of channel carriers |
| $V_{OX}$ | Voltage across gate oxide |
| $V_{GS}$ | Gate to source voltage |
| $V_{BS}$ | Body to source voltage |

## 2.2 FD-SOI Technology Description and Basic Equations

FD-SOI transistor is a planar device, as bulk's one, it means the gate control is a two-dimensional electrode. However, the structure is based on silicon thin film, in the range of a few nanometers ($\leq$10 nm actually) lying on a thin buried oxide ($\leq$50 nm). Macroscopic transistor scheme [3] is depicted in Fig. 2.1

Thin and fully depleted silicon film will decrease significantly the parasitic effect of the source and drain junctions on the channel area, enabling a stronger influence of the front gate. The benefit of the superior electrostatic control of the device in case of FD-SOI device is well explained by the concept of drain induced barrier lowering (the so-called DIBL). As shown in Fig. 2.2, the role of the source and drain region on the channel is directly related to the junction depth (labeled $x_j$). By shortening the physical gate related to Moore's law, we observed on increasing of the

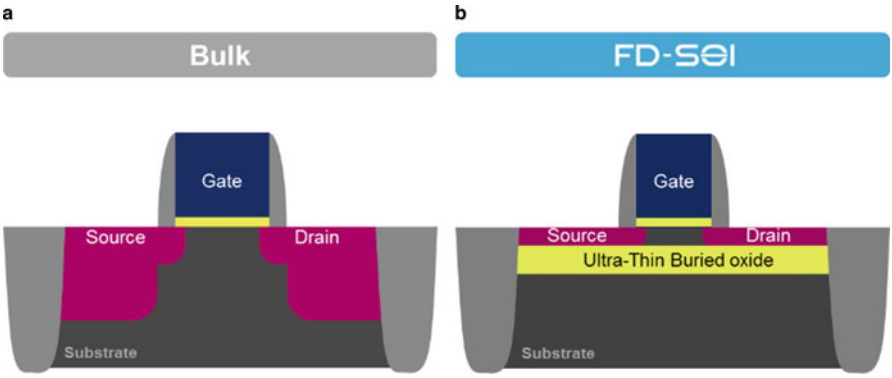


**Fig. 2.1** General structure evolution of CMOS transistor from bulk scheme (**a**) toward FD-SOI transistor (**b**)

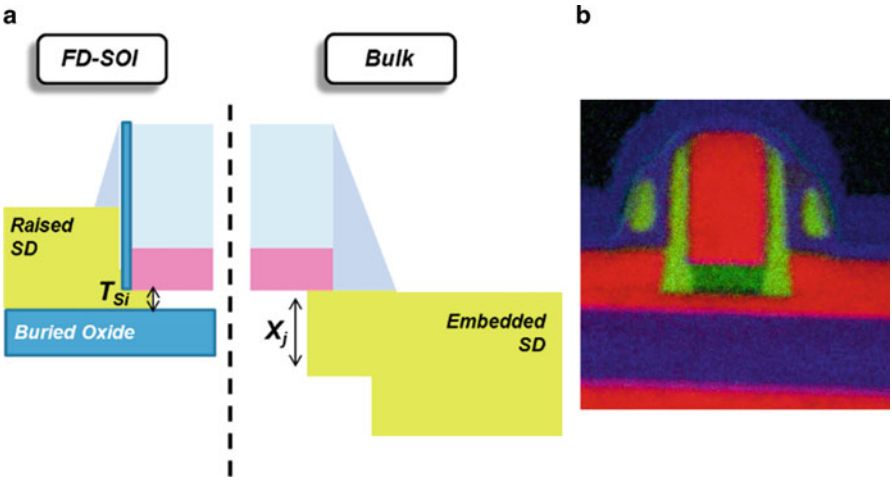


**Fig. 2.2** Junction design differences between bulk transistor, left side of (**a**) and FD-SOI one (**b**) influencing the electrostatic control and DIBL behavior

parasitic region controlled by junctions. Process wise, the scalability of the $x_j$ factor becomes more and more challenging because modulated by diffusion mechanism and consequently requiring very precise thermal budget at manufacturing side. To take into account such issue coming from the shrinkable, main parameter used to evaluate electrostatic performance of the transistor is $x_j/L_{\text{gate}}$ ratio. This ratio is exhibited in the $V_T$ Eq. (2.1) for short channel devices below [2].

$$\triangle V_T = \frac{qN_aW\left(\sqrt{1+\frac{2W}{x_j}}-1\right)}{C_{OX}} \cdot \frac{x_j}{L_{\text{gate}}} \tag{2.1}$$

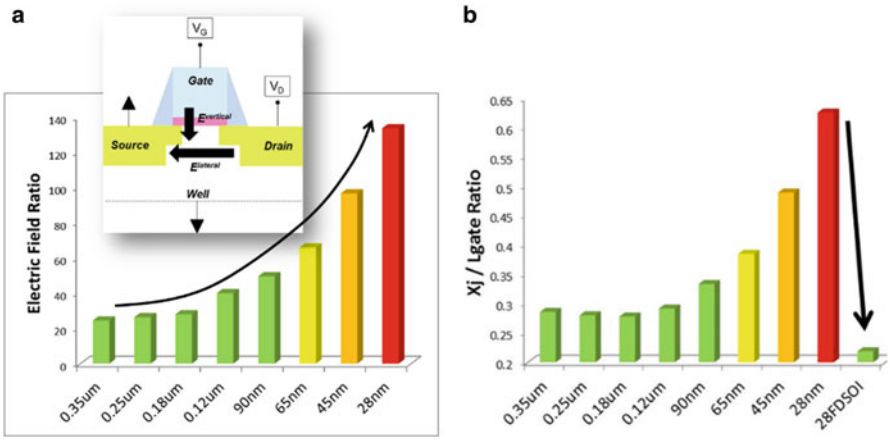


**Fig. 2.3** Challenge of electrostatic control of the channel in advanced CMOS technology due to the shrink of lateral dimension overcome thanks to FD-SOI architecture (**a**). $x_j/L_{\text{gate}}$ ratio significant improvement thanks to FD-SOI architecture (**b**)

In case of FD-SOI transistor, $x_j$ factor is replaced by the silicon film thickness, with much superior capability to be scaled down, because not driven by the physics of the diffusion. Thus, moving from mature CMOS technology to most advanced node, the difficulty to control the channel of the transistor has been overcome thanks to FD-SOI scheme (Fig. 2.3).

Circuit performance at low voltage is directly linked to the DIBL value of the device. Lower is the DIBL, higher is the low voltage performance. As shown by Eqs. (2.3) and (2.3), low DIBL requires low $x_j/L_{\text{gate}}$ ratio. In case of FD-SOI transistor, $x_j/L_{\text{gate}}$ ratio is replaced by $T_{Si}/L_{\text{gate}}$ [4].

$$DIBL_{\text{Bulk}} = 0.8.\frac{\epsilon_{Si}}{\epsilon_{OX}}\left(1+\frac{X_j^2}{L_{el}^2}\right).\frac{T_{OX}}{L_{el}}.\frac{T_{\text{dep}}}{L_{el}}.V_{DS} \tag{2.2}$$

$$DIBL_{\text{FD-SOI}} = 0.8.\frac{\epsilon_{Si}}{\epsilon_{OX}}\left(1+\frac{T_{Si}^2}{L_{el}^2}\right).\frac{T_{OX}}{L_{el}}.\frac{T_{Si}}{L_{el}}.V_{DS} \tag{2.3}$$

Aside the thin silicon film improving the control of the device, FD-SOI technology is based on thin buried oxide layer underneath the channel region. This thin oxide (<50 nm) allows a back side control of the channel. Well region play then the role of a back gate enabling a further biasing helping to create the inversion layer sooner. This pseudo-3D structure provides the opportunity for a back gate biasing as described in Fig. 2.4

Surface potential inside the channel represented by $\Psi$s parameter, depends on the metal work-function ($\phi$m) and the front gate biasing as expected in bulk transistor. Surface potential represents the status of the channel in terms of inversion layer, i.e., the availability of the device to transport carrier from source to drain region.

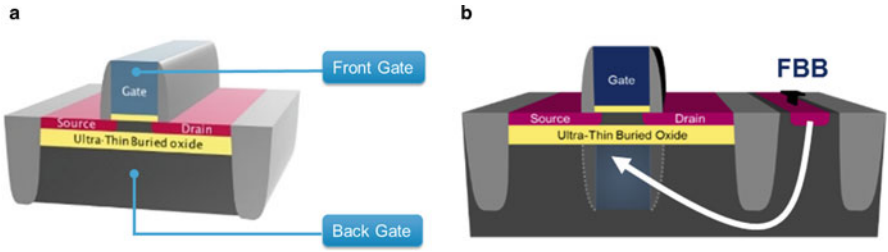


**Fig. 2.4** FD-SOI transistor double gate structure enabling FBB technique. **(a)** 3D structure of FDSOI transistor. **(b)** Back gate control of the device

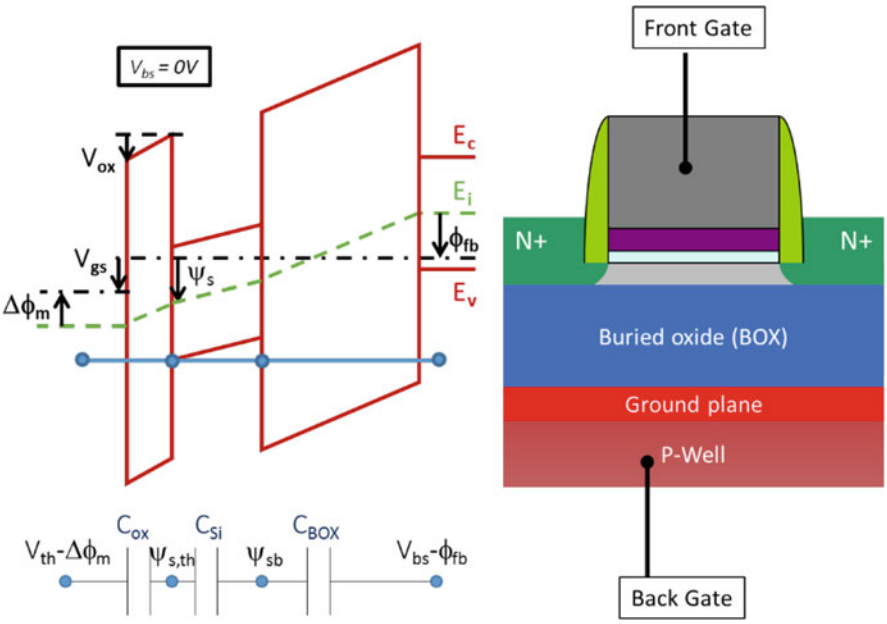


**Fig. 2.5** Back gate biasing effect on transistor band diagram modulating threshold voltage. ©IEEE 2017 reprinted with permissions

By applying a bias at the front gate ($V_{gs}$), $\Psi$s will increases and then free electrons will be generated in the channel. In the same way, a voltage applied at the rear of the buried oxide will modulate as well the surface potential, and the conduction channel. The setting and the adjustment of $\Psi$s will then depend on both front and back gate biasing ($V_{gs}$ and $V_{bs}$, respectively), as depicted in Figs. 2.5 and 2.6. Equivalent schematic is a coupling capacitance between $C_{OX}$ (front gate capacitance) and $C_{BOX}$ (back gate capacitance), the channel playing the role of an internal node. Morphological structure and band diagram illustrate this schematic [5].

This coupling allows a specific $V_T$ modulation without carrier mobility or junction leakage degradation. The FD-SOI transistor' $V_T$ equation is derived from bulk $V_T$ inversion capacitance,

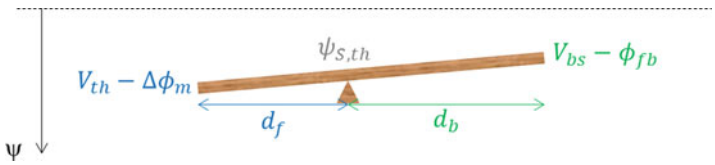


**Fig. 2.6** Surface potential equilibrium between the front gate materialized by $V_T$ and metal work-function and the back gate defined by body-bias and flat band voltage. ©2017 IEEE reprinted with permission

$$C_{\text{inv}} = C_{\text{dep}} + C_{OX} \tag{2.4}$$

Where in our case of full depletion,

$$C_{\text{dep}} = \frac{dQ_{\text{dep}}}{d\psi_S} = 0, C_{\text{inv}} = C_{OX} \tag{2.5}$$

From electrostatic potential:

$$C_{\text{inv}} = -\frac{dQ_{\text{inv}}}{d\psi_S} \tag{2.6}$$

$$C_{\text{inv}} = \frac{q \cdot n_i \cdot t_{Si}}{kT/q} \cdot e^{\psi_S/(kT/q)} \tag{2.7}$$

$$\psi_{S,th} = \frac{kT}{q} \cdot ln\left(\frac{C_{OX} kT/Q}{q n_i t_{Si}}\right) \tag{2.8}$$

Considering the creation of the channel at the front interface, the threshold voltage expression is obtained from the capacitive divider displayed in Fig. 2.6:

$$\frac{(V_T - \triangle\phi_m) - \psi_{S,th}}{1/C_{OX}} = \frac{\psi_{S,th} - (V_{bs} - \phi_{fb})}{1/C_{Si} + 1/C_{BOX}} \tag{2.9}$$

Posing:

$$BF = \frac{\partial V_{gs}}{\partial V_{bs}} \| \text{fixed } \psi_S$$

$$BF = \frac{1/C_{OX}}{1/C_{Si} + 1/C_{BOX}} \tag{2.10}$$

The capacitive coupling being denoted by BF factor depends on $C_{BOX}/C_{OX}$ ratio [5] and represents the gate voltage overdrive/underdrive brought by body-bias. From the ratio formula of BF in Eq. (2.10), we can predict that body-biasing will be more efficient in case of ultrathin buried oxide and thick oxide devices, as for I/Os and analog blocks.

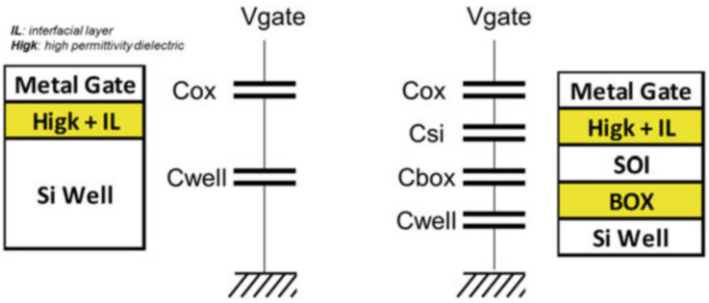


**Fig. 2.7** Vertical structure of MOS device in case of bulk-planar device (left) and FD-SOI one (right)

Finally, the threshold voltage expression is

$$V_T = \triangle\phi_m + \psi_{S,th} + BF \cdot (\psi_{S,th} - (V_{BS} - \phi_{fb})) + \frac{h^2}{8q \cdot m_{\text{conf}} \cdot t_{SI}^2} \tag{2.11}$$

where $m_{\text{conf}}$ represents the effective mass of confined carrier. The electrostatic behavior of the channel in case of FD-SOI device is different from what we use to observe in the case of the bulk-planar transistor. As described in Fig. 2.7, the vertical structure on FD-SOI transistor is completed by a pure coupling capacitance structure between the top oxide ($C_{OX}$) and the bottom one ($C_{BOX}$) and not by a depletion modulation.

The role of the coupling capacitance system inside FD-SOI scheme is represented in Fig. 2.8. We can model the evolution of the threshold voltage versus body-bias (here called $V_{bb}$). Since a reserve body-bias (RBB) is applied, the front channel is open, allowing a carrier transport at the front of Si channel. Channel conduction will shield the silicon film and then threshold voltage depends on $C_{BOX}/C_{OX}$ ratio. In case of a forward body-bias (FBB), a second inversion layer appears at the rear of the silicon film at Si/Box interface. It means that threshold voltage reduction depends on ($C_{BOX}$, $C_{OX}$, $C_{Si}$) triplet.

Under usual front gate polarization ($V_g = V_{dd}$ and $V_{bb} = 0$), inversion layer is generated only at the front gate interface as shown in red on Fig. 2.9 representing the charge density as a function of the position inside the silicon channel. If a RBB biasing is applied at the rear of the transistor, inversion charge is decreased corresponding to an increasing of threshold voltage. On the contrary, if a FBB is used at the back gate, a second inversion layer is observed at the Si/Box interface. This back conduction corresponds to a decreasing of the threshold voltage value of the transistor [6].

The charge density described above can be measured thanks to C-V characteristic of the MOS transistor. By changing the back gate voltage, we can modulate the

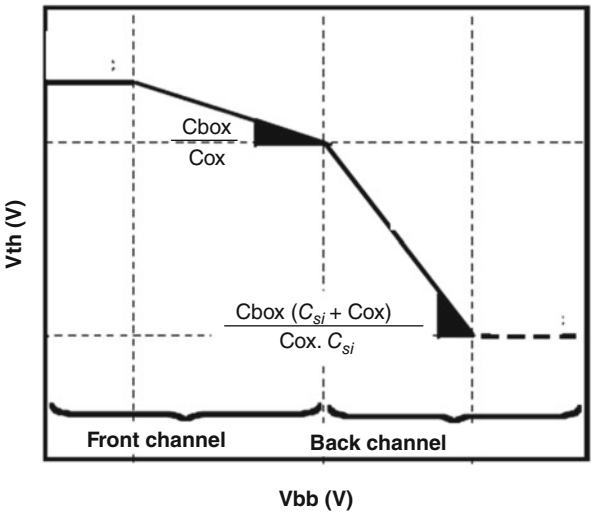


**Fig. 2.8** Threshold voltage evolution versus body-bias ($V_{bb}$) as a function of $C_{BOX}$, $C_{OX}$, and $C_{Si}$ coupling capacitances

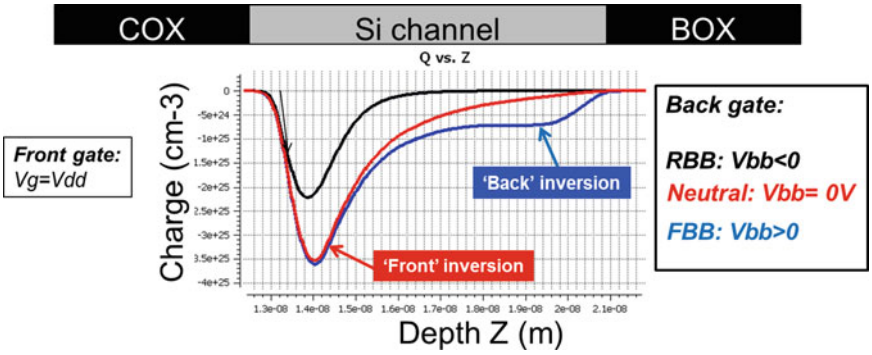


**Fig. 2.9** Charge density inside silicon channel versus back gate biasing (RBB, NBB, and FBB)

generation of the second inversion layer and then the vertical capacitance of the structure, as depicted in Fig. 2.10. For nominal condition ($V_{bb} = 0$ V) and RBB, a maximum capacitance corresponding to the $C_{OX}$ value is measured. It corresponds to a front conduction. In case of positive back biasing corresponding to FBB condition, and a back inversion layer appears dropping the capacitance value due to $C_{OX}$ in parallel with $C_{Si}$. Thus the shape of the C-V is influenced by the back gate if FBB is applied.

The fact to change the body-bias value, a significant change occurred for the sub-threshold regime. Main effects are represented in Fig. 2.11. As expected, $V_T$ goes up and down by applying negative or positive $V_{bb}$, respectively. As shown below, the sub-threshold slope is modulated by the body-bias as well. In the situation of RBB, we observed an improvement of the sub-threshold slope, as a sign of an improvement of the electrostatic control of the transistor. Actually, it can be explained by a better inversion layer localization under the front gate, as depicted