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Transaction-Level Power Modeling

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Preface

Transaction-Level Modeling (TLM) is a technique for building and developing designs. TLM introduces abstract modeling of communication schemes between design modules. It provides insights for system-level design at early stages of development. Thus, TLM accelerates the design cycle of System-on-Chip (SoC) in the industry.

A novel methodology, referred to as Transaction-Level Power Modeling (TLPM), is proposed. It is used to evaluate power consumption using TLM. Evaluating power consumption at early phases of product design cycle is important to decrease the number of expensive design iterations. The methodology exploits the existing tools for Register Transfer Level (RTL) simulation, design synthesis, and SystemC prototyping to provide fast and accurate power results. TLPM is performed in two stages: power characterization on RTL and power modeling on TLM. Experimental results reveal both efficiency and accuracy of the TLPM methodology. TLPM speeds up the simulation time by more than two orders of magnitude over RTL, while the error in power estimation is less than 3%.

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Abbreviations

AMBA	Advanced Microcontroller Bus Architecture
AP SoC	All Programmable SoC
APB	Advanced Peripheral Bus
AT	Approximately-time
CA	Cycle-Accurate
DMI	Direct Memory Interface
DUT	Design Under Test
EB	Energy per Byte
EMIO	Extended Multiplexed I/O
ESL	Electronic System Level
FPGA	Field-Programmable Gate Array
FRC	Free Running Counter
GL	Gate Level
GPIO	General Purpose I/O
GUI	Graphical User Interface
HDL	Hardware Description Language
HTLP	Hierarchical Transaction Level Power
HW	Hardware
I2C	Inter Integrated Circuit
IC	Integrated Circuit
LT	Loosely-timed
MIO	Multiplexed I/O
MISO	Master Input Slave Output
MOSI	Master Output Slave Input
OOP	Object-Oriented Programming
PKtool	Power Kernel Tool
PL	Programmable Logic
PPC	Performance Optimization With Enhanced RISC – Performance Computing
PS	Processing System

PV	Programmer View
PVT	Programmer View Plus Timing
RTL	Register Transfer Level
RXFIFO	Receiver First In First Out
SAIF	Switching Activity Interchange Format
SoC	System-on-Chip
SPI	Serial Peripheral Interface
SW	Software
TLM	Transaction Level Modeling
TLPM	Transaction Level Power Modeling
TXFIFO	Transmitter First In First Out
UART	Universal Asynchronous Receiver Transmitter
UPF	Unified Power Format
UVM	Universal Verification Methodology
VCD	Value Change Dump