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Parasitic Substrate Coupling in High Voltage Integrated Circuits

Minority and Majority Carriers Propagation in Semiconductor Substrate

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Foreword

In the early days, the high-voltage transistor was a discrete device, and the control and protection circuits were implemented with small ICs and discrete components. The interference between the circuits through common connections and supply lines was limited.

Due to rapid technology and packaging advancements, it became possible in the late seventies of the last century to integrate the high-voltage, high-power transistors with their protection and control circuits on the same chip: the Smart Power IC. This evolution is still ongoing with increasing power capability and switching speed of the power transistors and increasing accuracy and complexity of the protection and interface circuits on the same chip.

Most Smart Power ICs use junction isolation and increasingly suffer from interferences through the common substrate. Besides capacitive and inductive coupling between components, switching power devices also inject majority and minority carriers of considerable magnitude into the substrate. This gives rise to substrate biasing in the vicinity of the injection point and disturbance of sensitive interface circuits far away from the injection point.

The effects of these substrate currents are very difficult to predict since they propagate three-dimensionally through the substrate. Furthermore, traditional SPICE simulations only calculate with majority carriers and neglect minority carriers. Substrate couplings could hence not be included in the chip design cycle.

Traditionally, experimental test structures were used to quantify the substrate couplings in a given technology. Expert designers then devised circuit layout and protection structures with large margins to cope with the substrate interferences.

A much better and accurate approach is TCAD simulation of the whole chip. Such simulation includes the behavior of the minority carriers and the three-dimensional nature of the substrate current but requires tedious finite element modeling of the three-dimensional chip and lengthy simulations.

In this book, a new approach is presented. Equivalent electrical circuits are derived to model minority carriers in the substrate in SPICE, and a novel, meshing strategy is used to limit the number of nodes to model the chip layout. Together these advancements allow for simulation in SPICE of the parasitic substrate couplings in Smart Power ICs with adequate accuracy, and the simulation complexity is low enough to include critical layout interactions in the normal design cycle.

Herman Casier

Preface

Over the last century, electronics has been a major drive for the revolution in communication systems and in data computing. The demand for integrated circuits is accelerating as high integration of electronic functions is needed to share information and control our environment. The everlasting consumer demand for safety, energy efficiency, and connectivity explains why electronics is becoming of prime importance. In this context, the automotive industry is taking full advantage of this microelectronics revolution, and today, it happens to be one of the main users of integrated circuits.

Safety requirements for modern automotive electronics call for more and more robust circuits for power applications. In most situations, the mixed-signal circuit design flow cannot track ultimate design failures in complex power circuits mainly caused by parasitic substrate currents caused by majority/minority carriers. Traditionally, device simulations are carried out on a simplified model of the substrate to identify these parasitic signals. However, it is almost impossible to get accurate results with this approach. In addition, the circuit functionalities are excluded from these simulations since there is no back annotation between the substrate model and the circuit.

In this book, a novel substrate model and related extraction methodology is investigated. The substrate model consists in three generalized lumped elements—the EPFL diode, the EPFL resistor, and the EPFL homojunction—and a subdivision of the Integrated circuit (IC) layout into elementary cells where the continuity equation for the minority carriers is solved with the finite-difference method (FDM). A nonuniform mesh procedure is also implemented to minimize the number of nodes, giving rise to an equivalent three-dimensional model of the substrate. The concept is fully compatible with conventional circuit design tools, and it can be used for any high-voltage technology, including HV-CMOS and BCD processes. For instance, the single and parallel activation of substrate parasitic bipolar transistors in a 0.35 μm High voltage (HV) technology is verified with SPICE simulations, predicting the activation of a latch-up in specific situations. To address the general problem of reliability in IC design, a fast method to monitor parasitic substrate currents is also presented. The substrate analysis and identification of critical

substrate current path can be done during the preliminary design phase, allowing the placement of protections in an optimal layout floor plan.

This book can be used as reference for engineers and students designing HV ICs with high immunity to parasitic substrate current caused by the injection of minority and majority carriers. It is divided into seven chapters dealing with a specific aspect of the model or its applications.

Chapter 1 provides an overview of substrate coupling issues. The state of the art of modeling strategies, including minority and majority carrier propagation into the substrate, is presented, together with an overview of IC design flow showing the main open issues in parasitic coupling.

Chapter 2 focuses on the architecture of standard HV technologies, highlighting major causes and effects of parasitic substrate currents.

Chapter 3 details the mathematical derivation of the EPFL substrate model where equations are translated into equivalent enhanced devices in order to be solved by circuit simulators.

Chapter 4 analyzes the EPFL substrate model with respect to numerical device simulators, including DC, AC, transient, and temperature simulations. Finally, breakdown simulations of basic ESD devices are discussed and demonstrate the ability of the model to simulate snapback behaviors.

Chapter 5 describes the procedure developed to implement the substrate extraction tool still preserving back annotation with the circuit. A specific meshing and technology reduction methodology is also developed to simplify the extracted network.

Chapter 6 is the ultimate assessment of the model with respect to experimental data and discusses the performance in terms of simulation speed and memory storage.

Finally, in Chap. 7, a novel procedure is presented to simulate and control substrate currents aiming layout optimization. A survey of the most recent advances in designing passive and active isolation structures is also presented and analyzed in details with the model.

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Acronyms

ADAS	Advanced driver assistance system
BCD	Bipolar CMOS and DMOS
BJT	Bipolar junction transistor
CAD	Computer-aided design
CAN	Controller area network
CB	Common base
CE	Common emitter
CMOS	Complementary metal-oxide semiconductor
DI	Dielectric isolation
DMOS	Double-diffused MOS
DPI	Direct power injection
DRC	Design rule check
DSP	Digital signal processor
DTI	Deep trench isolation
EC	European community
ECGR	Electron-collecting guard ring
ECU	Electronic control unit
EDA	Electronic design automation
EMC	Electromagnetic compatibility
EME	Electromagnetic emission
EMI	Electromagnetic immunity
EPFL	Swiss Federal Institute of Technology of Lausanne
ERC	Electrical rule checker
ESD	Electrostatic discharge
FA	Failure analysis
FBM	Finite box method
FDM	Finite-difference method
FEM	Finite element method
GLD	Generalized lumped devices

HBM	Human body model
HCGR	Hole-collecting guard ring
HF	High frequency
HS	High side
HV	High voltage
IC	Integrated circuit
ISO	International Organization for Standardization
JI	Junction isolated
KCL	Kirchhoff's current law
KVL	Kirchhoff's voltage law
LCM	Line centered mesh
LDMOS	Lateral diffused MOS devices
LOCOS	Local oxidation of silicon
LS	Low side
LuT	Look-up table
LVS	Layout versus schematic
MAAP	Multi-ring active analogic protection
MCC	Minority carrier circuit
MCM	Minority carrier mirror
MOS	Metal-oxide semiconductor
MOSFET	Metal-oxide semiconductor field effect transistor
μP	Microprocessor
NCM	Node centered mesh
NFA	Negative feedback activated
NMOS	Negative-channel metal-oxide semiconductor
NPN	Negative-positive-negative (transistor)
NUM	Nonuniform mesh
PDE	Partial differential equation
PDK	Process design kits
PIC	Power integrated circuit
PWM	Pulse-width modulation
RC	Resistance and capacitance
RF	Radio frequency
SCR	Silicon-controlled rectifier
SI	Self-isolated
SNS	Sah-Noyce-Shockley
SOA	Safe operating area
SOAC	Safe operating area check
SoC	System-on-chip
SOI	Silicon-on-insulator
SPT	Smart power technology
SRAM	Static random-access memory
SRH	Shockley-Read-Hall

SVE	Smart voltage extension
TCAD	Technology computer-aided design
TCC	Total current circuit
TLM	Transmission line model
TVS	Transient voltage suppressor
UM	Uniform mesh
VDMOS	Vertical diffused MOS

Chapter 1
Overview of Parasitic Substrate Coupling

1.1 Substrate Parasitic Current

In an IC, electrical couplings between analog and digital circuits take place through minimal impedance paths between the metal interconnections layers and the substrate. Concerning metals, the parasitic contributions generated by resistances and capacitances can be directly obtained from the layout. Concerning the semiconductor substrate, the situation is much more complex since both majority and minority carriers currents come into play and the minimum impedance paths are not easily identified.

Electrical parasitic coupling between analog and digital circuits in mixed-signal designs is commonly referred as *substrate noise*. In industrial and automotive applications, additional parasitic currents are generated by the switching of inductive loads or by stringent ESD and Electromagnetic compatibility (EMC) tests. For instance, a significant injection of minority carriers (electrons in a p-type substrate) in substrates occurs when power MOSFETs driving an inductive load are switched off. In this situation, the drain voltage of the power transistor is suddenly biased below the substrate potential, and the parasitic substrate Bipolar junction transistor (BJT) is activated.

The injected minority carriers generate a reverse substrate current that can be collected by n-type wells of digital and analog circuits nearby. Moreover the reverse current flow can be of hundreds of milliamperes and can generate a latch-up, which is the most disruptive effect that can be triggered by an injection of minority carriers.

In general, three kinds of substrate current can be identified, each of them having different characteristics and mitigation strategies [1, 2]. Here, a p-type substrate is considered.

- **Majority carriers current:** when a parasitic PNP transistor is activated, it injects majority carriers into the substrate, thus generating a substrate potential shift (de-biasing). The substrate acts as a distributed collector for the parasitic BJT,

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and the de-biasing becomes dependent on the equivalent bulk resistivity. Proper P+ grounding schemes are required to reduce these potential shifts;

- **Minority carriers current:** when the parasitic device is a NPN transistor, minority carriers are injected into the substrate and generate currents that interact with surrounding n-wells. Now, the substrate holds for the distributed base of a parasitic multi-collector BJT. The presence of additional n-wells and the layout floor planning have a huge impact in the resulting coupling currents;
- **Switching noise current:** AC currents from fast switching transistors can also couple through junction capacitances, generating high-frequency noise and substrate potential spikes. In this case the substrate acts as a distributed RC network, and the contact placements, as well as decoupling capacitors, are needed to mitigate the induced noise.

The first two types of substrate current are those generated in power stages of HV ICs when PN junctions of HV MOSFETs are forward biased and start injecting electrons (minority carriers) or holes (majority carriers) into the substrate. These charges can disturb nearby circuits and, in the worst case, can destroy the chip if a latch-up is triggered. Then, it is essential to adopt effective strategies at the circuit level (e.g., proper timing of transistor control signals) and during the layout stage (e.g., using appropriate guard rings and proper floor planning). However, no model is available to predict these parasitic signals during the design of the circuit.

Moreover, these kinds of couplings depend on the substrate doping as well. HV technologies require low doping in order to increase breakdown voltages. At the same time, low-doped substrates mean long minority and majority carrier's lifetimes and diffusion lengths. In this case, parasitic currents can generate coupling mechanisms far in the IC. To fix this issue and force recombination, a P++ highly doped substrate can be used together with a p-epi layer.

Concerning the switching noise generated during AC operation, it is attributed to capacitive coupling phenomena driven by the junction capacitances, in contrast to substrate current from bipolar transistors that are DC contributions. Switching noise is generated by high-frequency operation of digital and mixed-signal circuits, but still it is a source of noise for sensitive analog or RF cells [3]. This kind of substrate coupling can be easily modeled with a distribute RC network [4] as shown in Fig. 1.1 where a power stage, a logic block, and a sensitive bandgap circuit are placed nearby. Here the aggressor is the fast switching logic, and the noise detected depends on the equivalent impedance of the substrate [5]. But when the power stage is activated, meaning that a DC current sinks in a parasitic multi-collector structure, the RC modeling approach is unable to predict the induced shift in the bias voltage of the bandgap circuit (the selected victim) [6, 7]. In any case, during the switching of the power MOSFETs, AC and DC contributions coexist and must be taken into account.

In order to suppress substrate switching noise, the RC time constant must be increased by introducing grounding schemes and decoupling capacitances. Also in this case, the doping of the substrate has an influence since it fixes the resistance of the bulk [8]. For low-doped substrates, the resistivity is high, and the noise is

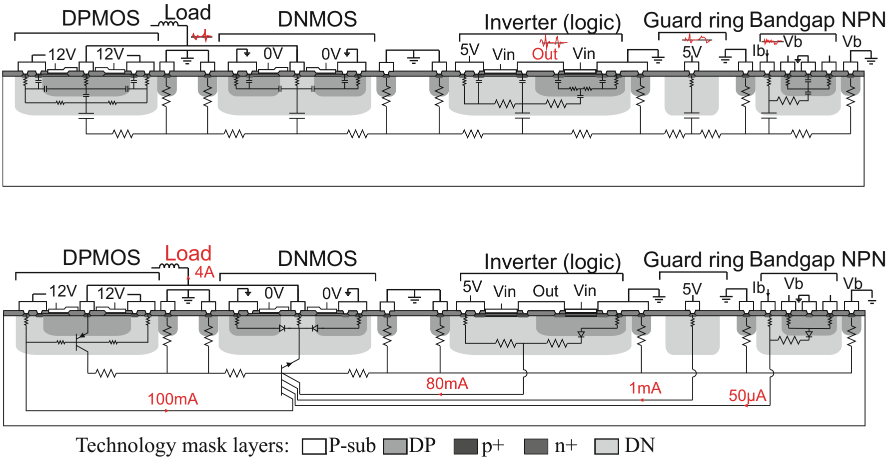

Fig. 1.1 Cross section showing impedance paths of substrate couplings: (top) switching noise from an inverter and (bottom) belowground condition of a H-Bridge injecting current into the substrate. In the first case, the n-well acts as a decoupling capacitor, while in the second case, it behaves as an additional collector for the parasitic NPN BJT device

decreased by increasing the distance between the noisy elements and the sensitive circuits. For high-doped substrates, the P++ bulk propagates the noise “uniformly” across the chip, and the distance has a negligible impact. However, in this case the resistivity is lower and also the overall RC noise.

1.2 Electrical Modeling of the Substrate: State of the Art

The coupling related to a parasitic NPN BJT is very dependent on the distance between emitting and collecting wells in the layout. There is no reliable compact model to simulate parasitic currents generated by these parasitic BJTs since the current gain β of a lateral NPN BJTs depends on the 3D layout configuration. Foundries may provide additional layout guidelines to avoid or reduce substrate coupling currents. Additionally, measurements of BJTs are done to estimate the sensitivity of parasitic signals to the layout [9, 10]. This is done by injecting a current I_E into the substrate and measuring the collected current I_C from different collector nodes. It results in some empirical fitting curves for the parameter $\alpha = I_C/I_E$ that is used to quantify the substrate couplings. Still, such results cannot be generalized for multi-collector or multi-emitter configurations due to the nonlinearity of minority carrier’s current propagation. Finally, depending on the layout, additional coupling mechanisms are competing, and these are almost impossible to predict with a predefined BJT model.

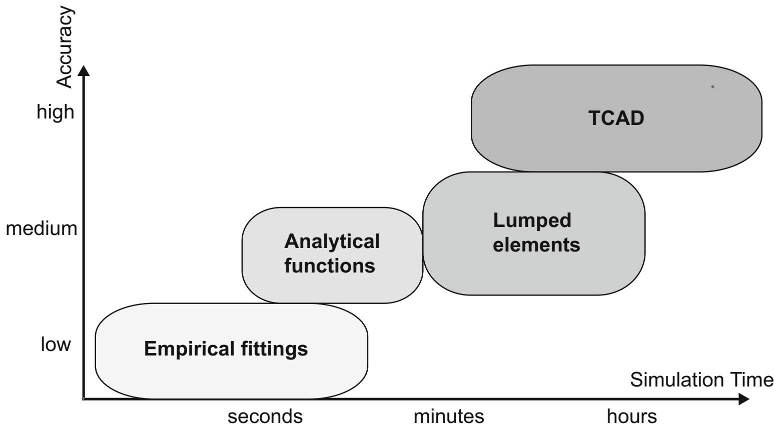

Fig. 1.2 Comparison of different substrate modeling methodologies

Different substrate modeling methodologies are compared in Fig. 1.2. The accuracy refers to the predictability of the model with respect to different layouts and electrical configurations. As expected, Technology computer-aided design (TCAD) software is the most accurate to simulate the substrate current since transport equations are solved numerically. However, this requires lots of computer resources and long simulation time and cannot be extended to a full IC. In this context, TCAD has been used to analyze substrate couplings in HV circuits like a H-Bridge [11] once the technology parameters are properly calibrated [12]. Then, co-simulation of mixed-signal design flow and TCAD as proposed by Gnani et al. [13] happens to be the most accurate solution to analyze substrate current coupling. Still, one drawback is the lack of back-annotation between the "selected" piece of substrate in TCAD and the original circuit schematic. A solution was proposed by Kollmitzer et al. [14] where TCAD is used to characterize minority carriers couplings and to create a model that can be included into the original circuit by the means of Look-up tables (LuTs). However, to ensure accuracy, a new TCAD simulation is required each time a different layout is analyzed.

Other numerical techniques have been exploited to reduce the simulation time down to seconds. One is to use Green's function to solve the diffusion equation of minority carriers [15]. This option requires a complex mathematical formulation that can hardly include drift currents, a serious limitation under high electric fields. Moreover, it cannot be integrated directly in circuit simulators.

This is the strategy adopted by Oehmen et al. [16]. In their approach the substrate is divided into spheres, and the diffusion equation is solved in polar coordinate satisfying Kirchhoff's laws. The equation is solved in each single sphere to calculate the injected electrons concentration, while the coupling currents are computed as linear combinations of all minority carriers' densities. Nevertheless, this methodology still focuses on the diffusion of minority carriers, neglecting drift current components and majority carriers (e.g., the vertical PNP BJT cannot be simulated with this approach).