ACSP · Analog Circuits And Signal Processing

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Self-powered SoC Platform for Analysis and Prediction of Cardiac Arrhythmias

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Preface

During the last decades, medical wearable devices have gain lots of interest due to their potential influence in providing remote and ambulatory monitoring to support patients. Many devices have been developed, improved, and implemented for the long-term and continuous monitoring of the healthcare practices in general and cardiovascular diseases in particular. Due to its efficiency, simplicity, and noninvasiveness, the electrocardiogram (ECG) signal has been widely used for monitoring cardiac functions despite the development of newer techniques or technologies. The information contained in the morphological features of the ECG signal has been broadly employed to build a full classification system capable of distinguishing between normal and abnormal conditions.

This book presents the first ASIC implementation of an ECG-based signal processor (ESP) that is capable of predicting ventricular arrhythmia up to 3 h before the onset. The ESP is composed of three stages which include ECG signal processing, feature extraction, and classification, and it utilizes adaptive and novel techniques that are highly effective and suitable for real-time implementation. The extracted ECG features, individually and in combinations, showed good potential in the prediction of ventricular arrhythmia with significant statistical results, and the combination of these features has never been used in any previous detection or prediction system. Two databases of heart signal recordings from MIT PhysioNet and the American Heart Association (AHA) were used as training, test, and validation sets to evaluate the performance of the proposed system. Based on MATLAB testing results, the proposed system achieved a prediction accuracy (ACC) of 99.98% on the out-of-sample validation data by tenfold cross validation with 3-s window size.

Furthermore, the proposed ESP was developed using Verilog RTL and implemented using ASIC implementation flow based on 65-nm GlobalFoundries

low-power CMOS process. Based on the design constraints, the ESP occupied a state-of-the-art total cell area of 0.112 mm^2 and consumed a total power of 2.78 μW at an operating frequency of 10 kHz and operating voltage of 1.2 V.

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We also like to acknowledge the support of Mubadala for the funding and the US Semiconductor Research Corporation (SRC) for overseeing the projects of the ACE4S Mubadala-SRC Center of Excellence under which this project was completed. We must also acknowledge our industrial liaisons for their suggestions and insights, John Pigott, Mark Schlarmann from NXP, Muhammad Khellah, and Lilly Huang from Intel.

The work in this book was part of a complete system on chip targeting a platform for wearable healthcare. We would like to thank our colleagues responsible for other parts of such a system and acknowledge their unmatched spirit of teamwork. Finally we would like to acknowledge the help and support of our families and friends and thank them for their patience and understanding.

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