Dr. B. Vinoth Kumar
Dr. K.N. Vijeyakumar
K. Saranya

Single Precision Floating Point Multiplier

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ABSTRACT

The Floating Point Multiplier is a wide variety for increasing accuracy, high speed and high performance in reducing delay, area and power consumption. The floating point is used for algorithms of Digital Signal Processing and Graphics. Many floating point multipliers are used to reduce the area that perform in both the single precision and the double precision in multiplication, addition and subtraction.

The scientific notations sign bit, mantissa and exponent are used. The real numbers are divided into two, fixed component of significant range (lack of dynamic range) and exponential component in floating point (largest dynamic range). Converting decimal to floating point and normalize the exponent part and rounding operation for reducing latency. The mantissa of two values are multiplied and adding the exponent part. The sign result with exclusive-or are obtained. The final result of shift and add floating point multiplier is compared with booth multiplication. From the synthesis it is observed that shift and add floating point multiplier performs 20% better in different parameters such as delay, area and power is verified by Verilog Hardware Description Language. These results are also verified in Cadence EDA tool.

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